Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Yokohama, 2006, pp. 1026-1027

G-8-4

High Performance SiN-MIM Decoupling Capacitors with Surface-smoothed Bottom Electrodes for High-speed MPUs

Ippei Kume, Naoya Inoue, Hiroto Ohtake, Shinobu Saitoh, Naoya Furutake, Jun. Kawahara, Takeshi Toda*, Toshiki Shinmura*, Koujirou Matsui*, Takayuki Iwaki*, Koichi Ohto*, Masayuki Furumiya* and Yoshihiro Hayashi

System Devices Research Laboratories, NEC, and *NEC Electronics
1120 Shimokuzawa, Sagamihara, Kanagawa 229-1198, Japan
Phone: +81-42-771-4267 Fax: +81-42-771-0886 e-mail: kume@mel.cl.nec.co.jp

Abstract Ultra-thin SiN MIM decoupling capacitor (DCC) has been developed in the Cu BEOL with high capacitance up to 7 fF/μm^2. The surface property of the polycrystalline-TiN bottom electrode (BE) affects SiN dielectric reliability, and the smoothed surface by thin Ta insertion improves TDDB reliability by approximately 6000 times.

1. Introduction

To suppress power-line noises of high-speed MPUs [1], Metal-Insulator-Metal (MIM) capacitor in the Cu-BEOL, instead of MIS capacitors with large leakage currents through the extremely thin gate-oxide, is needed as decoupling capacitors (DCC). Thin SiN film with k~7[2] is a candidate for the dielectric of the MIM because of high process compatibility with the current LSI fabrication. However, capacitance of the previously reported SiN MIM is limited to ~2 fF/μm^2 [3], which is not sufficient for the latest MPUs (Table 1).

In this work, ultra-thin SiN film was employed to obtain large capacitance over 5 fF/μm^2. In order to improve dielectric reliability, the surface property of the polycrystalline-TiN bottom electrode is discussed.

2. Experimental

Figure 1(a) shows the illustration of the SiN-MIM capacitor, in which both top and bottom electrodes are connected to the upper power/ground lines. As shown also in Fig. 1(b), effects of the surface property of the polycrystalline TiN bottom electrode (BE) were investigated from the viewpoint of the etching controllability as well as the MIM characteristics. Sputtering process deposited 140 nm-thick TiN BE, followed by deposition of 15 nm-thick, microcrystalline-Ta film to smooth the BE surface. Then, PECVD-SiN films of 3 to 15 nm thicknesses were deposited, and 100 nm-thick TiN top electrode (TE) was also sputtered. After etching the TE electrodes with Cl_2-based gases, the MIM capacitors of 1680 μm^2 were integrated into the Cu-DDI (Fig. 2). The capacitance @100 MHz, the leakage current, V_{BD} and TDDB were evaluated for the integrated SiN MIMs.

3. Results and Discussion

(a) MIM profile control:

After etching the TiN TE on the 10 nm-thick SiN, the resultant surface of the TiN BE suffered from severe roughening (Fig. 3(a)). Ultra-thin SiN on the TiN BE was partially etched away during the over-etching, and the remained SiN acted as micro-masks to the TiN BE due to the high etching rate of TiN to SiN (Fig. 4(a) and Table 1). Insertion of Ta, which had high selectivity in etching rate to TiN, behaved as an excellent etching stopper, resulting in the smooth surface of the BE after TE etching as shown in Figs. 3(b) and 4(b). Thus, the Ta/TiN BE improves the MIM etching profile with ultra-thin SiN.

(b) Electrical Properties:

Figure 5 plots capacitance of the SiN MIMs as a function of surface roughness of the BE under the SiN film. Here, the roughness was controlled by thickness of the polycrystalline TiN BE. Capacitance increased with the surface roughness in both cases of the TiN and Ta/TiN BEs. Increase of capacitance with roughness is related to geometric increment of the effective surface area. TEM images and AFM profiles (Fig. 6) proved that the surface roughness of BE was smoothed by deposition of Ta on the TiN BE. Note that discrepancy of capacitance between TiN and Ta/TiN BEs in Fig. 5 was originated from the difference in the incubation time of the SiN deposition designed for the 10nm-thickness, or essentially from actual SiN thickness. Hereafter, the SiN thickness is expressed as the actual thickness measured.

In natural, leakage current and capacitance increased with decreasing SiN thickness (Fig. 7). For the ultra-thin SiN below 10 nm, Ta insertion effectively reduced leakage current due to surface smoothing effect. The conduction mechanism of 10 nm-thick SiN on Ta/TiN was confirmed to be P-F mode, which was also observed in the relatively thick SiN (13 nm) on TiN. (Fig. 8) Fig. 9 shows relation of leakage current and capacitance for the SiN MIM structures after full integration. We successfully fabricated the SiN MIM with high capacitance and low leakage current using the Ta/TiN BE. The results demonstrated that the SiN MIM-DCC is applicable in the capacitance of 7 fF/μm^2.

(c) MIM Reliability: Reliability was tested for the MIM capacitors with or without Ta insertion. Insertion of Ta on the TiN BE improved the breakdown characteristic of the 10 nm-thick SiN MIM with 7 fF/μm^2 (Fig. 10), achieving high breakdown field of 6 MV/cm, which was much higher than that of the thick SiN (13 nm) on TiN BE with 5.5 fF/μm^2. Fig. 11 shows the dependence of $t_{63.2}$ in the Weibull plot of TDDB test, shown in the inset, on the stress bias (E-filed). Insertion of Ta improved TDDB lifetime by approximately 6000 times due to reduction of the roughness of the BE.

4. Conclusions

Coverage of the TiN BE with thin Ta layer achieves excellent controllability of etching process of the MIM structure with ultra-thin SiN. In addition, insertion of the Ta layer reduces the surface roughness of the polycrystalline-TiN BE, and the smoothed surface improves the dielectric characteristics such as leakage, breakdown and TDDB reliability in the integrated MIM capacitors. The SiN-MIM with the Ta/TiN BE achieves high capacitance of 7 fF/μm^2, along with longer TDDB lifetime by approximately 6000 times than that without Ta insertion.

Acknowledgements

The authors would like to thank Dr. Sekine, Dr. Yamazaki, and Dr. Kuwata at NECEL and Dr. Mochizuki and Dr. Sumihiro for their support and technical discussions.

References

1) N. Inoue, To be presented in IITC2006 (2006).
2) T,Remmel, et al, Rel. Phys. Symposium Proc., pp573-574,(2004)
3) R. Liu, et al, IITC2000, pp111-113, (2000).

Table 1 Characteristics of SiN MIM

SiN MIM Properties	This work	7fF/μm² 10^{-9}A/cm²@1.6V (10nm)
	Reported [2,3]	~2fF/μm² 10^{-10}A/cm²@5V (~30nm)
Etching selectivity	TiN/SiN	~6
	SiN/Ta	~0.4
	TiN/Ta	~15
Etching Gases		Cl_2,BCl_3,Ar,CHF_3
Equipment		Compatible with conventional line
Line contamination		None

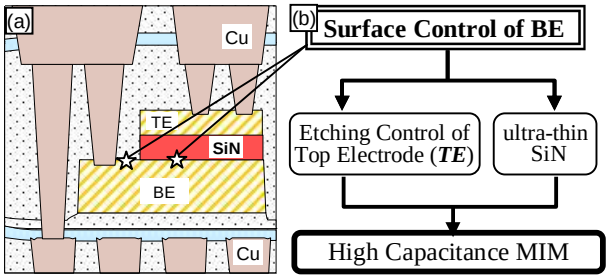


Fig.1 Ultra-thin SiN- MIM capacitor integrated into the Cu BEOL; (a) illustration and (b) technical points of this work.

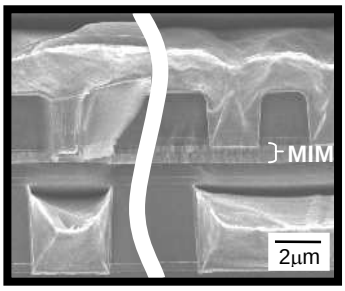
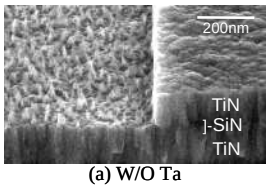
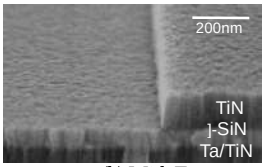


Fig.2 SEM image of the Ultra-thin SiN MIM fabricated.



(a) W/O Ta



(b) With Ta

Fig.3 SEM images of the etched surface after TE etching (a) without and (b) with Ta thin layer.

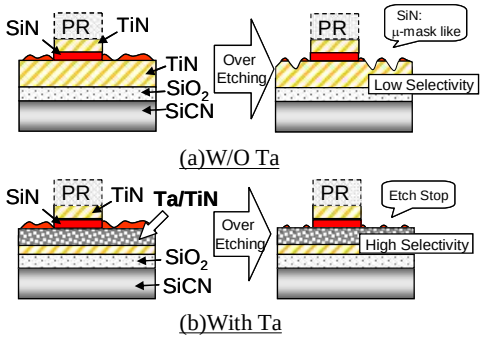


Fig.4 Effect of over-etching during TE etching (a) without and (b) with Ta thin layer on the TiN BE.

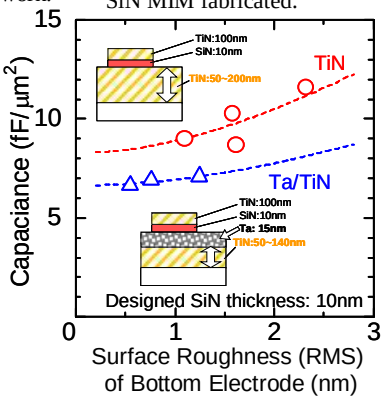


Fig.5 Dependence of capacitance on the surface roughness of BE.

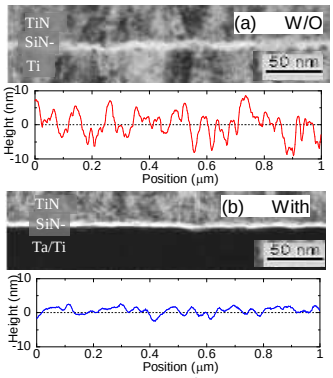


Fig.6 XTEM images of MIM structures and surface profiles of the BEs (a) without and (b) with Ta thin layer.

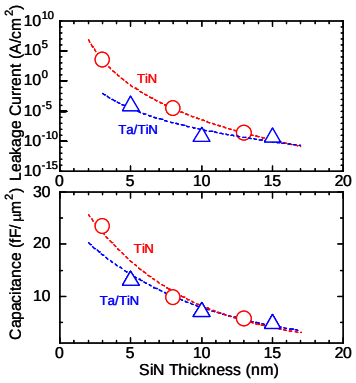


Fig.7 Leakage current and capacitance as a function of the SiN thickness.

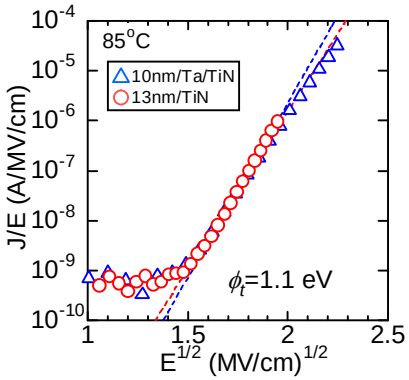


Fig.8 P-F analysis of the leakage current of the integrated capacitors.

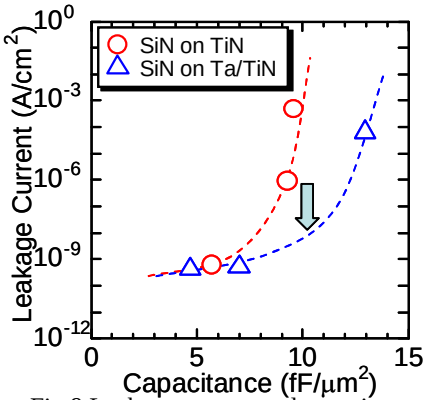


Fig.9 Leakage current and capacitance of the SiN MIM capacitors. Insertion of Ta on TiN BE reduces leakage current, especially in high capacitance region.

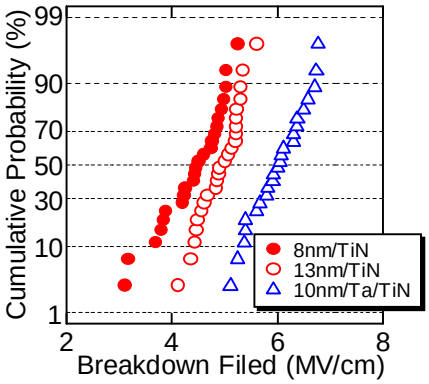


Fig.10 Cumulative probability of breakdown field for the SiN MIM capacitors with TiN or Ta/TiN BEs.

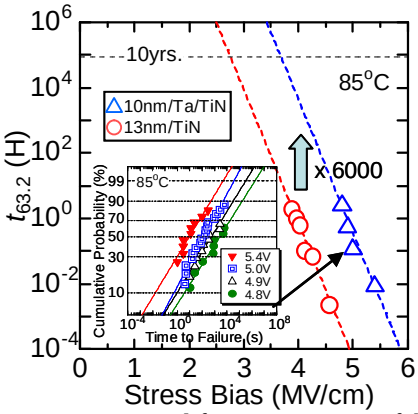


Fig.11 TDDB lifetime estimation of the capacitors with TiN or Ta/TiN BEs. Inset is the Weibull plot for capacitors with Ta thin layer.