Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Yokohama, 2006, pp. 1028-1029

G-9-1 (Invited)

Reliability challenges for advanced copper low-k interconnects

Zs. Tőkei[1], C. Bruynseraede[1], Y-L. Li[1,2], I. Ciofi[1], G.P. Beyer[1]

[1]IMEC, Kapeldreef 75, 3001 Leuven, Belgium
[2]Dept. of Electrical Engineering, Katholieke Universiteit Leuven, 3001 Leuven, Belgium
e-mail: zsolt.tokei@imec.be; Tel: ++32-16-281778 - Fax: ++32-16-281214

1. Introduction

Looking towards the 32 nm technology node and beyond the introduction of novel materials is probably required along with scaling of dimensions in order to ensure the necessary performance and partly address power consumption challenges. Providing sufficient reliability margin for aggressively scaled copper low-k interconnects is a major integration and reliability challenge. In this contribution the associated reliability challenges will be addressed through state-of-the art case studies. The methodologies include time dependent dielectric breakdown (TDDB), triangular voltage sweep (TVS), electromigration (EM) and stress induced voiding (SIV).

2. Dielectric Reliability

TDDB testing is often used for assessing the reliability of advanced copper low-k damascene interconnects. While the methodology gained fast acceptance, the relevant mechanisms and models are still being debated. It is reported that the dielectric reliability margin is shrinking with each technology node and in turn the relevance of TDDB testing increases. Because of design, material choice, virtually all damascene process steps and the integration method do affect the TDDB performance, it is systematically used for characterization of the integrated dielectric quality. In Fig. 1 the TDDB performance of SiOC:H based dielectrics is plotted as function of porosity using the same integration method [1] for fabricating 80/80 nm width/spacing meander comb structures. When porosity increases the apparent reliability margin is degraded by several orders of magnitude. Contributors such as the CMP interface on dense dielectrics, the barrier/dielectric interface on porous dielectrics and/or low-k dielectric modification during the integration are relatively well documented [2-5].

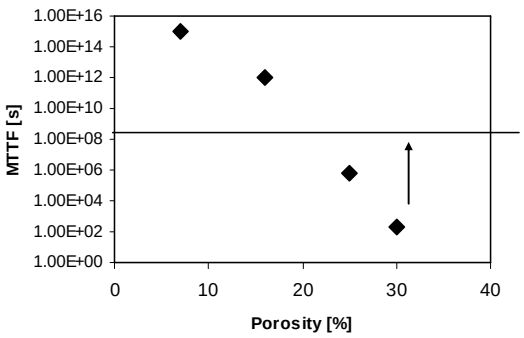

Fig.1 TDDB lifetime is significantly shorter if the same integration method is used for porous materials.

Historically, copper diffusion barrier performance was among the first challenges to tackle and accordingly, several of the existing models describing damascene dielectric degradation deal with copper [6,7]. Experimental evidence shows that if copper is incorporated/injected into a dielectric stack during processing or reliability testing it causes drastic lowering of the breakdown strength. The degradation is often so severe that the presence of copper is unlikely to be tolerated. But even mature schemes have decreased TDDB lifetime for reduced spacing, which cannot be explained by copper presence. Defect free metallic and dielectric diffusion barriers remain to be very important, but considering copper as a sole possibility for fast degradation is not appropriate. Lately plenty of attention has been paid to dielectric modification of the low-k materials and to densification and/or incorporation of moisture into these modified regions. Dielectric modification and moisture uptake deserves attention not only for preserving the benefit of applying a low-k material, but also because it significantly impacts dielectric reliability. As the spacing decreases the relative importance of these modified areas becomes increasingly important. As several investigations show [3,5,8-11], dielectric modification and moisture uptake do influence leakage currents and breakdown strength, because it induces non-homogenous defect and field distribution. Fig.2 illustrates that the 100 ppm lifetime rapidly decreases if spacing values are approaching to the 32 nm technology node dimensions. Though, data are available the understanding is far from complete. Complementary techniques are required in order to better characterize the integrated dielectric quality. Many of the to-date proposed methods involve either blanket layer characterization or special sample preparation, which may not be representative of the integrated dielectric.

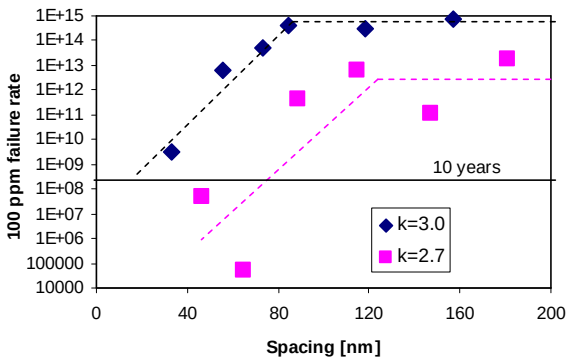

Fig.2 100 ppm failure rate at 100 °C for SiOC:H materials versus dielectric spacing

The TVS method can, however, be directly applied on damascene lines without special sample preparation. The method enables both the detection of copper and moisture due to characteristic features in the TVS trace [12,13]. It is an indispensable technique for deeper understanding the cause for fast degradation and failure. Fig. 3 shows a TVS trace recorded from a 16 % porosity SiOC:H damascene structure, where the humps superimposed onto the capacitor displacement and leakage currents were identified as being moisture related.

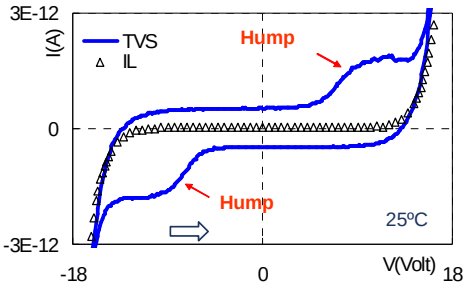

Fig.3 TVS leakage current for a 16% porosity SiOC:H damascene structure

3. Metal reliability

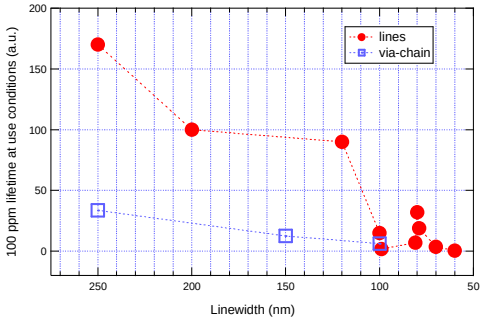

Fig. 4 Loss of EM performance upon line and via scaling. All lifetimes are extrapolated to the same user condition

Metal reliability is generally assessed by studying EM and SIV. In the case of EM the physical models are much more mature than for example for TDDB testing. While the physical understanding of copper wire degradation mechanisms is less of a debate, technological challenges towards the fabrication of metal wires/vias able to carry the ever increasing current densities are enormous. This is illustrated in Fig. 4, where EM lifetime is shown as a function of line/via dimensions. Process improvements can partly restore reliability margins, but with the increasing prevalence of vulnerable interfaces those alone may not be able to cope with the ever increasing current densities if materials are kept unchanged. The dominant interface for EM failure is in most cases the Cu/cap interface. Improving adhesion does improve EM lifetime, but does not change the physics for degradation. Introducing novel cap materials, which reduce surface mobility by several orders of magnitude (e.g. CoWP caps), drastically improves the strong mode EM performance (Fig. 6). It is noted that non

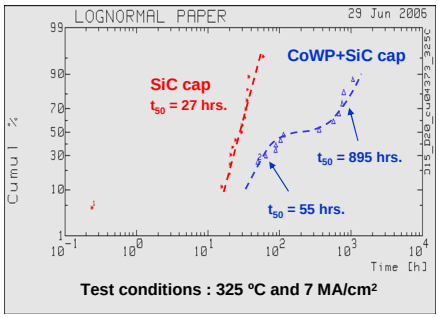

Fig. 6 CoWP cap layer can significantly improve EM

optimal selectivity can lead to extrinsic EM failures (Fig. 6) and also compromise dielectric reliability through leakage current increase and degraded TDDB performance. Careful optimization for all reliability aspects is therefore necessary. Another avenue for improving the metal reliability is by alloying copper itself with a solute element that decreases interface and grain boundary vacancy migration either by strong interaction or simply by occupying the energetically most favorable sites. Fig. 7 shows the result of SIV for a dual damascene SiOC:H via-line structure into which a diluted copper-aluminum wire was implemented.

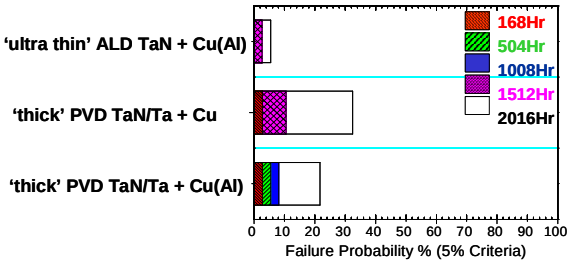

Fig.7 Alloying results in reduced Cu and vacancy diffusion along Cu/barrier and grain boundary interfaces. A non-blocking via-bottom barrier further reduces SIV failure rate.

4. Conclusions

For advanced copper low-k integration both metal and dielectric reliability are of crucial importance. For the 32 nm node and beyond significant progress was made in the understanding of the associated failure mechanisms. Successful integration schemes should eliminate dielectric modification and reduce interfacial metal and vacancy migration.

References

[1] H. Struyf et al., IITC (2005) 30.
[2] J. Noguchi et al., IRPS (2000) 339.
[3] Zs. Tőkei et al., AMC (2005) 687.
[4] Zs. Tőkei et al., IRPS (2004) 326.
[5] Zs. Tőkei et al., IRPS (2005) 495.
[6] W.Wu et al. IRPS (2003)
[7] F. Chen et al., IRPS (2006) 46.
[8] F. Iacopi et al., MRS 2004 F.1.5.
[9] D. Edelstein et al. IRPS (2004) 316
[10] Y. Travaly et al., ADMETA (2005) 12.
[11] A. Ikeda et al., IITC (2006) 42.
[12] I. Ciofi et al., MRS (2006) accepted for publication.
[13] I. Ciofi et al., IITC (2006) 181
[14] C. Bruynseraede et al. IRPS (2005) 7.