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# An Excellent Cu Diffusion Barrier for Next Generation Multi-level Cu-interconnect

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**Abstract**

A new Cu diffusion barrier of TaPt alloy with excellent performance is proposed. The TaPt film remains nearly amorphous after 800°C annealing and exhibits excellent Cu barrier ability up to 650°C under bias-temperature stress at 2MV/cm and 200ºC for 60 min. Low resistivity, good adhesion, high Cu(111) orientation, and good thermal stability make it a promising Cu diffusion barrier.
Keywords: Cu-interconnect, diffusion barrier, TaPt alloy

## Introduction

Since the first demonstration of Cu-interconnect in 1997, it becomes the main stream for multi-level metallization of high performance integrated circuits [1]. High quality metallic Cu diffusion barrier is one of the key factors for successful Cu-interconnect. The barrier metal must satisfy several requirements including good Cu barrier ability, low resistivity, high Cu(111) texture preference, good thermal stability, and good adhesion to Cu seed and inter-metal dielectric. Several materials have been proposed as next generation barrier metal [2-5]. Unfortunately, none of them can meet all of these requirements simultaneously. Therefore, Ta/TaN stack is still expected to be used in the near future.

In this work, we propose an excellent Cu diffusion barrier of TaPt alloy. Both the film properties and Cu barrier ability are examined thoroughly. By incorporating Pt into Ta, all of the requirements can be satisfied.

## Experiments

Simple MOS capacitors with gate electrode of TaPt(5 or 20 nm) /Cu(200nm)/TaPt(5 or 20 nm) were fabricated. The gate oxide is a 60nm thick thermal oxide. The TaPt alloys were deposited in a co-sputtering system. The sputtering power of Ta and Pt targets were set to DC 30 watt and RF 30 watt, respectively. The Cu layer was also deposited by sputtering. The alloy gate was patterned by lift-off process. Blanket TaPt(50nm)/$SiO_2$/Si samples were also prepared for TaPt thin film characterization.

## Results and Discussion

*A. TaPt Thin Film Characteristics*

The Ta/Pt atomic ratio determined by RBS is about 85/15. Fig.1 shows the XRD spectra of the TaPt film after annealing at various temperatures. The weak and broaden signal indicates that the film remains amorphous even after 800ºC annealing for 30 min. The main phase is supposed to be σ phase according to the phase diagram [6]. Fig.2 shows the cross-sectional TEM micrograph of the 800ºC annealed 50 nm thick TaPt film. Only few nano-crystals can be observed. The diffraction pattern also confirms the nearly amorphous state. Fig.3 shows the resistivity of the TaPt film after annealing at various temperatures. The resistivity of Ta film and TaN film are also shown in the figure. The incorporation of Pt does not increase the resistivity and the resistivity is stable up to 800°C.

Stud-pull adhesion test indicates that the adhesion of TaPt to $SiO_2$ is stronger than 50 MPa and is as good as that of Ta to $SiO_2$. Since Ta exhibits good adhesion to the porous carbon doped oxide (CDO), it is believed that the TaPt alloy should have similar behavior, too [7]. Good adhesion is also observed on the Cu/TaPt stack.

*B. Cu diffusion barrier properties*

Fig.4 shows the AES depth profile of the TaPt(20nm)/Cu(200nm)/TaPt(20nm) structure before and after 600ºC annealing for 30 min. No Cu diffusion into the TaPt barrier is observed. Fig.5 shows the high frequency C-V characteristics of the TaPt(5nm)/Cu/TaPt(5nm) MOS capacitors after annealing at various temperatures. The slight distortion after annealing at temperatures higher than 400°C is attributed to the stress induced interface states. The almost overlap of the C-V curves after 500, 600, 650, and 700 ºC annealing implies that Cu atoms can be blocked by the 5 nm thick TaPt barrier layer effectively. Fig.6 shows the flatband voltage ($V_{fb}$) as a function of annealing temperature. The tight distribution and small deviation confirms the TaPt barrier ability. Fig.7 shows that the breakdown voltage of the 650ºC annealed samples is similar to that of the 400ºC annealed ones. A 700ºC annealing results in low breakdown voltage. The minority carrier lifetime in Si substrate is also evaluated by the retention time measurement. The almost identical retention times shown in Fig.8 indicate that the Si substrate is not contaminated by Cu up to 650ºC.

Finally, a strong bias-temperature stress (BTS) test at 2MV/cm and 200ºC was performed. Figs.9, 10, and 11 show the C-V characteristics of the 600ºC, 650ºC and 700ºC annealed samples, respectively. For the 600ºC and 650ºC annealed samples, with 5 nm thick TaPt, BTS for 30 min and 60 min do not result in $V_{fb}$ shift. The 700ºC annealed sample, with 20nm thick TaPt, can not pass this strong BTS test.

Fig.12 compares the XRD spectra of the TaPt/Cu/TaPt and the Ta/Cu/Ta sandwich structure after 500ºC annealing for 30 min. The Cu(111)/Cu(200) intensity ratios of the TaPt sample is very close to that of the Ta sample. This result implies that the Cu-interconnect reliability with TaPt barrier should be similar to that with the current Ta/TaN stack barrier.

## Conclusions

TaPt alloy exhibits excellent quality as Cu diffusion barrier. It remains amorphous after 800ºC annealing and exhibits excellent Cu barrier ability under 700ºC furnace annealing. The 650ºC annealed sample can sustain BTS at 2MV/cm and 200ºC for 60 min. Together with low resistivity, good adhesion, and high Cu(111) texture preference, it is suggested that the TaPt alloy would be the most promising barrier metal for next generation Cu-interconnect technology.

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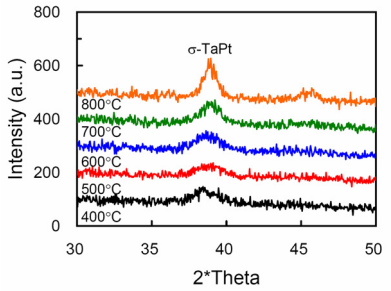


Fig.1 XRD spectra of the TaPt alloy after furnace annealing at various temperatures for 30 min.

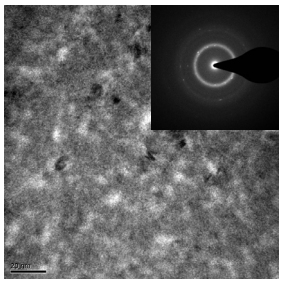

Fig.2 Plane-view TEM micrograph of the TaPt alloy after furnace annealing at 800ºC for 30 min.

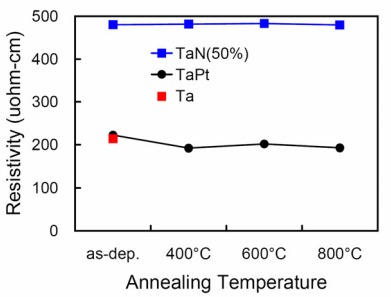


Fig.3 Resistivity of the TaPt alloy after furnace annealing at various temperatures for 30 min.

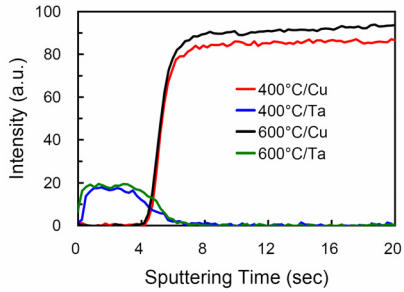


Fig.4 AES depth profile of the TaPt/Cu/TaPt stack after annealing at 400ºC and 600ºC for 30min.

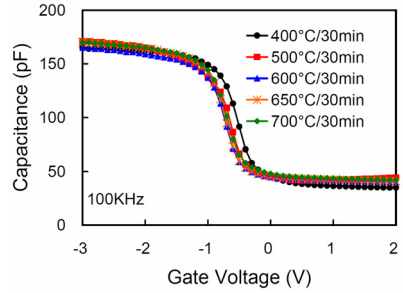


Fig.5 C-V characteristics of the MOS capacitor after annealing at various temperatures.

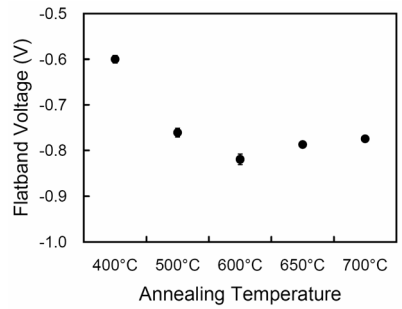


Fig.6 Flatband voltage of the MOS capacitor after annealing at various temperatures.

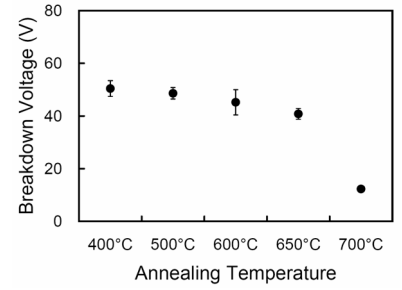


Fig.7 Absolute value of breakdown voltage of the MOS capacitor after annealing at various temperatures.

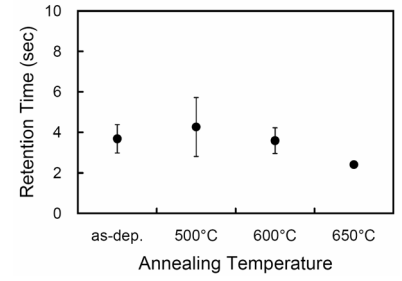


Fig.8 Retention time of the MOS capacitor after annealing at various temperatures.

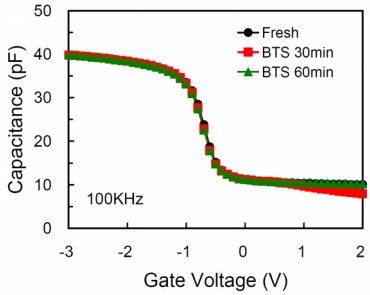


Fig.9 C-V characteristics of the 600ºC annealed sample before and after BTS at 2MV/cm and 200ºC.

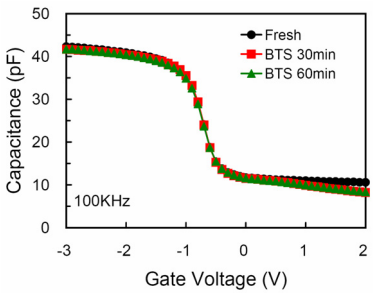


Fig.10 C-V characteristics of the 650ºC annealed sample before and after BTS at 2MV/cm and 200ºC.

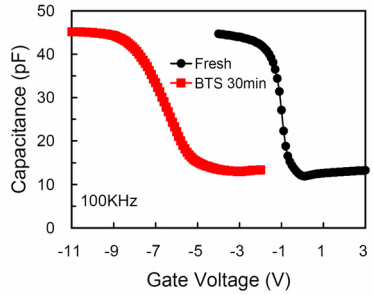


Fig.11 C-V characteristics of the 700ºC annealed sample before and after BTS at 2MV/cm and 200ºC.

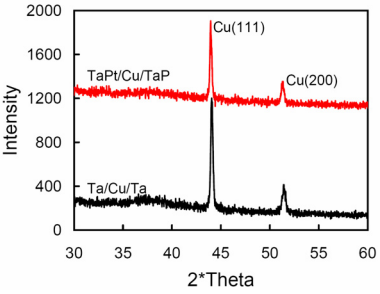


Fig.12 XRD spectra of the TaPt alloy after furnace annealing at 500ºC for 30min.