Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Yokohama, 2006, pp. 160-161

H-1-1 (Invited)

Direct Silicon Bonded (DSB) Mixed Orientation Substrate for High Performance Bulk CMOS Technology

C.Y. Sung, Haizhou Yin*, H. Ng*, K. L. Saenger, G. Pfeiffer*, V. Chan*, R. Zhang*, J. Li*, J.A. Ott, R. Bendernagel*, S.B. Ko*, Z. Ren*, X. Chen*, V. Ku*, Z.J. Luo*, N. Rovedo*, K. Fogel, M. Khare, G. Shahidi and S. Crowder*
Research Division, T.J. Watson Research Center, Yorktown Heights, NY 10598
* Semiconductor Research & Development Center
Microelectronic Division, Hopewell Junction, NY 12533

Abstract

This paper review the newly developed high performance bulk CMOS technology using the direct silicon bonded (DSB) substrates and the amorphization-templated recrystallization (ATR) technique. We review DSB substrate fabrication methods, interfacial oxide layer dissolution scheme, ATR process implementation, defect removal study, bonding interface quality monitoring, and superior PFET performance on (110) orientation. More than 20% faster ring oscillator speed was demonstrated by introducing minimal extra process steps to achieve nFETs on (100) and pFETs on (110).

Introduction

The concerns of CMOS scaling limits and device performance drive research interest in new materials (e.g., high-k gate dielectrics and metal gates) and new substrates (e.g., strained Si substrate, ultra thin SOI).[1,2,3] Mixed orientation substrates enable CMOS technology to be fully benefited from the highest hole and electron mobility on (110) and (100) Si orientation respectively.[4,5,6] DSB substrates are bulk like and therefore still compatible with the bulk CMOS processes and designs. The ATR technique[7] requires only minimal extra steps (implantation and annealing) to selectively convert nFET region from (110) to (100) and to keep the blocked pFET region with its the original (110) orientation. DSB technology is attractive for its simplicity and excellent performance.

Direct Silicon Bonded Substrate (DSB) Fabrication

A (110)-orientated silicon layer is directly bonded to a (100)-orientated Si-based substrate by hydrophobic (H-terminated surfaces) or hydrophilic (OH-terminated, oxide-like surfaces) bonding (Fig.1a). Hydrophilic bonding is widely used to produce silicon-on-insulator wafers. Since DSB substrate requires an interfacial SiO2 layer thickness as close to zero (Fig.1b) for the orientation changing ATR, the hydrophobic bonding is preferred. However, due to the H-terminated surfaces attracting particulates interfering with bonding, the hydrophobic bonding is more difficult and less widely practiced. The desired top 110 layer thickness, which can be inferred from the fringe spacing in high resolution x-ray diffraction[6], is controlled by thermal or mechanical cleave. The long wavelength oscillations from reflectance spectra (which DSB wafers does not show) usually indicate the bonding interfacial oxide (Fig.2). A unique high temperature anneal is developed to dissolve the interfacial oxide after bonding (Fig.3a). XTEM show the interfacial SiO2 disappear from bonding interfaces after anneal. Fig.3b SIMS indicates an oxide free interface.

Amorphization-Templated Recrystallization (ATR)

ATR uses Si^+ or Ge^+ ions[7,8] for amorphization with the energy(Si^+ ~100keV, Ge^+ ~220keV), angle (7° tilt) and dose (Si^+ 2E15, Ge^+ 2E15) for 2000A DSB to enable complete amorphization from the top surface to a depth below the bonding interface. Figs.4a,b show the amorphized layer, the damaged crystalline layer and the end-of-range (EOR) implanted ion loops. Templated recrystallization is performed at temperatures 650-900°C for 10 mins to recrystallize the amorphous layer to the orientation of underlying handle wafer and no bonding interfaces remain. EOR defects can be further removed by an additional long high temperature 1300 °C anneal (Fig.4c).

To implement ATR for CMOS device fabrication, the selected nFET regions for an orientation change are amorphized by ion implantation and then recrystallized to the base substrate (100) orientation with or without STI (shallow trenches isolation) in place. The masked unimplanted pFET regions remain the original (110) orientation. The recrystallization rate is fastest in (100) and slowest in (111) orientation. STI bounded trench-edged defects[8,9] originated from the poorest SPE on (111) planes starting a the three-phase intersection of the amorphous/crystalline interface and the existing STI trench edge during recrystallization. In Fig.5 a, the top down SEM showing STI bonded trench-edge defects. The cross section XTEM shows 110/100 lateral interface defects after ATR (the left of Fig.5. (b)). To avoid the above challenge, it is preferred to implement ATR without STI in place and use STI trench etch later to remove defects at 110/100 lateral orientation boundaries.[10] (the right of Fig. 5(b)). The final CMOS structure cross section XTEM is shown in Fig.5(c) and Fig.6a. The pFET on (110) orientation, nFET on ATR converted (100) without the original bonding interface are confirmed by the electron diffraction patterns. The topdown DSB XTEM indicates that defect-free SRAM nEFT regions can be achieved.

Device Performance

65-nm technology bulk CMOS devices are fabricated on conventional bulk (100) and DSB substrates with ATR and compared with (100) and (110) bulk substrates controls without ATR. nFETs fabricated on the ATR converted (100) on DSB and ATR'd bulk (100) are essentially identical to those fabricated on the (100) bulk controls without ATR. pFETs fabricated on the ATR implant blocked (110) on DSB are identical to those fabricated on the (110) bulk controls without ATR. ATR successfully converts (110) to (100) on nFETs without compromising pFETs device performance.

The nFETs from (100) bulk and DSB with ATR show the same drive current as those in (100) controls: 1000μA/μm at I_{off}=40nA/μm, 35% higher than the (110) control[6]. The DSB pFETs show 32% in isolated devices and 44% in nested devices drive current enhancement as compared to the (100) controls at I_{off}=5nA/μm. DSB also shows less degradation (only 3%) from the isolated to nested devices compared to (100) controls with 11% degradation (Fig.7). Functional unloaded ring oscillators on DSB with ATR are more than 20% faster in speed relative to the (100) controls with and without ATR (Fig.8). The pFETs Ion vs Ioff characteristics on DSB like their 100 controls show no width dependency (Fig.9). Meanwhile nFETs and pFETs overlap capacitance are the same for (100), (100) and DSB with ATR (Fig. 10). Special gate oxide processes are developed to achieve substrate orientation independent growth for thin and thick gate oxides. ATR processes do not degrade the channel surface quality which is indicated by the nitrided gate oxide same leakage current (Toxgl) and Tinv on all substrates, with and without ATR (Fig. 11). Well isolation healthiness is measured by breakdown voltages shown in Fig.12. P+ to P well, N+ to N well and N+ to N+ well are the same for (100) with ATR, DSB with ATR, the (100) and (110) controls. Therefore, the dopant diffusion properties and dependence of breakdown voltage are not impacted by ATR. However, the P+ to P+ leakage which differs from others because is sensitive to the bonding interface quality and ATR process conditions. The NiSi, diffusion sheet resistances, threshold voltage and linear Ion characteristics for short and long channel devices all show no degradation from ATR on DSB[6].

Conclusions

High performance bulk CMOS technology using the direct silicon bonded (DSB) substrates and the amorphization-templated recrystallization (ATR) is successfully demonstrated on 65nm technology. We reviewed the highly manufacturable DSB substrate fabrication, an unique interfacial oxide layer dissolution scheme, the cost effective ATR processes and defect removal methods, the bonding interface quality of material and device studies and showed that DSB pFETs Ion vs Ioff performance improved by more than 30%(isolated)-40%(nested devices). By introducing minimal extra steps to DSB substrate, nFETs on (100) and pFETs on (110) easily achieve more than 20% faster ring oscillator speed. DSB technology is attractive for its simplicity and high performance.

References

[1] S.C Song et al., VLSI Tech Dig. P. 2.4 (2006).
[2] K. Rim et al., IEDM Tech. Dig. p. 51 (2003).
[3] D. Singh et al., IEDM Tech. Dig. p. 511 (2005).
[4] T. Sato, et al., Jpn. J. Appl. Phys. **8**, p.588 (1969).
[5] M. Yang et. al., IEDM Tech. Dig. p.453 (2003).
[6] C.-Y. Sung, et al., IEDM Tech. Dig. Paper 10.3 (2005).
[7] K.L. Saenger et al., Appl. Phys. Lett. 87, p. No. 221911 (2005).
[8] K.L. Saenger et al., Mater. Res. Soc. Symp. **810**, C4.19.1 (2006).
[9] N. Burbure et al., Mater. Res. Soc. Symp. **810**, C4.19.1 (2004).
[10] H. Yin et al.,unpublished.

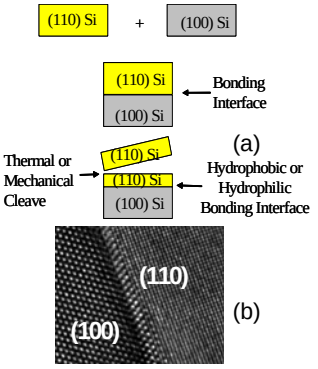


Fig.1(a) Direct Si bond (DSB) mixed orientation substrate fabricated by either hydrophobic or hydrophilic bonding. (b) XTEM shows no interfacial oxide.

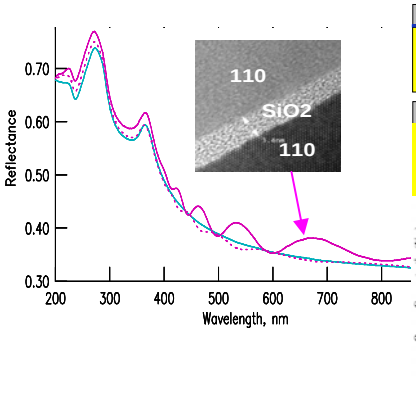


Fig.2. The long wavelength oscillations (pink curve) in reflectance spectra indicate the 2-3nm interfacial SiO2 layer at bonding interface (see XTEM). The blue curve is from bulk and DSB wafer.

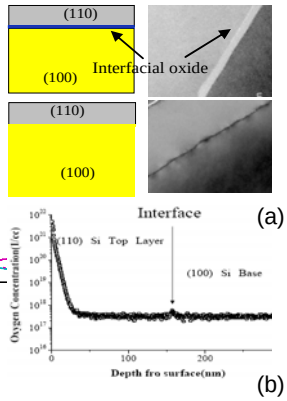


Fig.3. (a)XTEMs show bonding interfaces before and after high temperature interfacial oxide dissolving anneal. (b)SIMS indicates an oxide free interface.

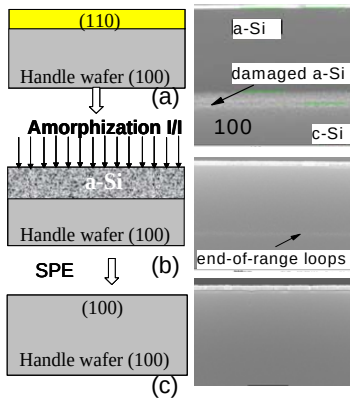


Fig.4. ATR on (100) Si. (a) The amorphized layer in an implanted sample. (b) After recrystallization anneal a-Si converted to (100) with end of range loops (EOR), c-Si (c) EOR disappear after defect removal anneal.

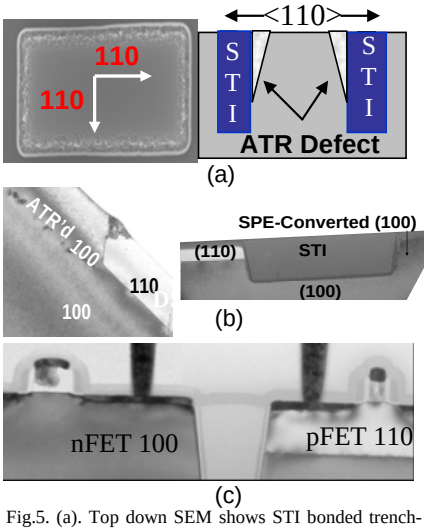


Fig.5. (a). Top down SEM shows STI bonded trench-edge defects. (b) Left: Cross section XTEM shows 110/100 lateral interface defects after ATR. Left: 110/100 lateral interface defects are etched away by STI trench etch. (c) Final CMOS structures.

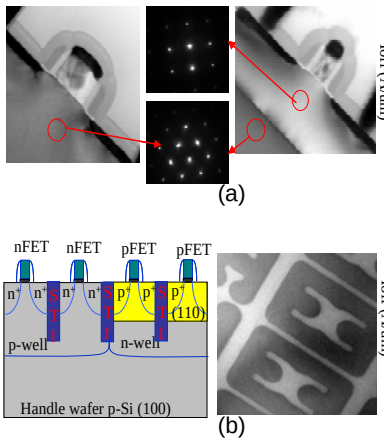
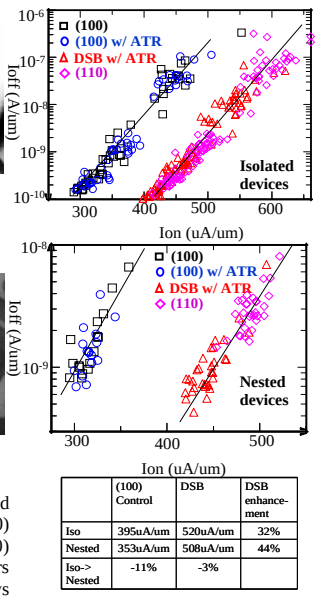


Fig.6. (a) The cross section XTEMs and diffraction pattern confirm pFET on (110) orientation, nFET on ATR converted (100) orientation. The bonding interface disappears thru ATR. (b) The top down XTEM shows defect-free SRAM NEFT region.



	(100) Control	DSB	DSB enhance-ment
Iso	395uA/um	520uA/um	32%
Nested	353uA/um	508uA/um	44%
Iso-> Nested	-11%	-3%	

Fig.7. PFET Ion vs. Ioff comparison between the isolated/nested devices and DSB/(100) control. DSB shows less degradation from the isolated to nested devices and more enhancement from 32% (iso) to 44% (nested) at Ioff 5nA/um.

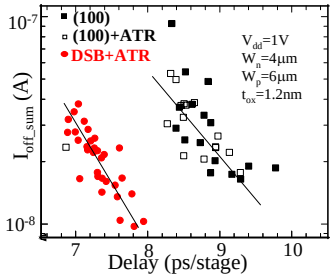


Fig.8. DSB+ATR achieve more than 20% faster ring oscillator speed.

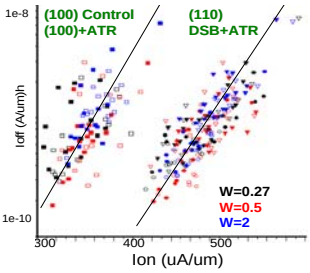


Fig.9. Both DSB PFET and 100 control show width independence of Ion vs Ioff .

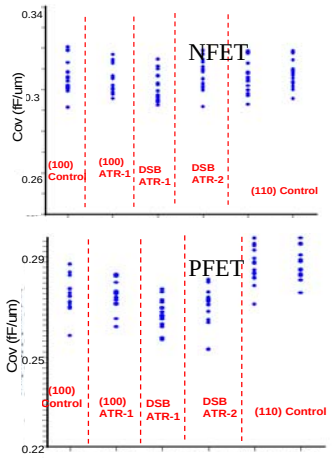


Fig.10. Overlap capacitance measured on (100), (110), (100) with ATR and DSB with ATR show similar values.

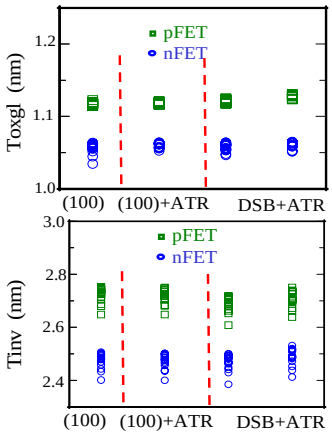


Fig.11. Both N/P FETs on DSB and 100 control show the thin/thick gate oxide growth rates orientation independence benefited by the new GOX processes.

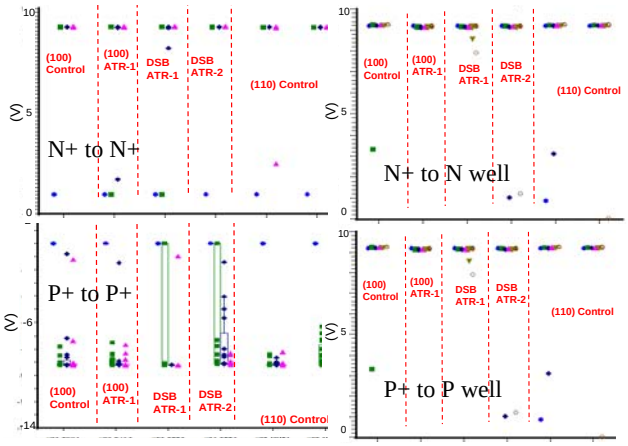


Fig 12. Well isolation measured by breakdown voltages. The P+ to P+ leakage differs from P+ to P well, N+ to N well and N+ to N+ well is sensitive to bonding interface quality and ATR process conditions.