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Sub-30 nm Strained P-Channel FinFETs with Condensed SiGe Source/Drain Stressors

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ABSTRACT

We report the first demonstration of strained p-channel FinFETs with SiGe source and drain (S/D) regions formed by a Ge condensation process. The novel local Ge condensation not only drives the Ge profile into the Si fin and/or increases the Ge concentration in the S/D regions for enhanced strain effects, but also eliminates the need for S/D recess etch, leading to process simplicity. Compared to a FinFET with uncondensed $Si_{1-x}Ge_x$ S/D, FinFETs with condensed $Si_{1-y}Ge_y$ S/D exhibit 28% higher drive current. Devices with gate lengths down to 26 nm were demonstrated with excellent control of short-channel effects.

INTRODUCTION

FinFETs or multiple-gate transistors offer superior control of short channel effects and therefore enable better scalability than planar transistors beyond the 32 nm technology node. In addition, there is immense interest to increase the transistor speed or drive current I_{Dsat} performance through carrier mobility enhancement using strain [1]. Recently, compressively strained p-channel FinFETs with $Si_{0.8}Ge_{0.2}$ source/drain (S/D) stressors were demonstrated [2], achieving an I_{Dsat} enhancement of 25% over control FinFETs. The integration of recessed SiGe S/D in FinFETs for hole mobility enhancement faces several challenges, particularly for SiGe S/D with high Ge concentration and for aggressively scaled devices with narrow fins. Furthermore, to enhance the strain effects, SiGe should also be grown on the fin sidewalls near the S/D regions, requiring the removal of poly-Si and spacer stringers prior to SiGe epitaxy.

In this work, we report the demonstration of sub-30 nm tri-gate FinFETs with SiGe S/D formed using a novel local condensation process. The Ge condensation [3] eliminates the need for a recess etch which is particularly difficult for aggressively scaled FinFET devices. In addition, the Ge concentration in the SiGe S/D can be increased for enhanced strain effects, and could enable the scalability of strain to unprecedented levels in pFETs.

DEVICE FABRICATION

The process flow for the fabrication of p-channel FinFETs with SiGe S/D is detailed in Fig. 1. Three device structures fabricated in this work are depicted in Fig. 2(a), including a control FinFET, a strained FinFET with elevated SiGe S/D, and a strained FinFET with recessed SiGe S/D using the local condensation process. Silicon-on-insulator (SOI) substrates with 40 nm thick Si were used as the starting materials. Threshold voltage V_t adjust implant was performed. Fin patterning employed 248 nm lithography, resist trimming, and reactive ion etching (RIE) to achieve fin widths W_{fin} down to 30 nm. Sacrificial oxidation was performed to repair the fin sidewall damage due to the RIE. SiO_2 gate dielectric (~3 nm) was thermally grown, followed by poly-Si gate deposition. Sub-30 nm gate lengths were achieved. The silicon nitride (SiN) spacer formation process ensured complete removal of SiN stringer at the base of the fin sidewall, therefore enabling full exposure of fin sidewall and top surfaces for selective SiGe growth to maximize the strain effects.

Selective epitaxial growth of $Si_{0.75}Ge_{0.25}$ was performed on all wafers except the control wafer. Fig. 2(b) shows a three-dimensional schematic of a portion of a FinFET with the fin and S/D region completely wrapped by the SiGe epi-layer. On one device structure with SiGe S/D, Ge condensation was performed. A cross-section through the SiGe-covered Si fin [plane in dashed lines in Fig. 2(b)] is shown in Fig. 2(c). When Ge condensation or oxidation was performed on a SiGe-covered Si fin, Si atoms from the SiGe are oxidized to form an oxide while Ge atoms are driven into the S/D regions of the fin [Fig. 2(c)]. S/D implant and anneal was performed to complete the fabrication process.

RESULTS AND DISCUSSION

In Fig. 3, stress simulation using Taurus Process shows a larger compressive strain along the channel direction for an embedded (top and both sides) SiGe S/D having a recessed depth of 5 nm. TEM images of test structures before and after Ge condensation are shown in Fig. 4. Diffractogram [Fig. 4(a) inset] shows the excellent epitaxial quality of SiGe. A 950°C 20 min Ge condensation, essentially an oxidation process, drove the Ge atoms into the Si fin [Fig. 3(b)]. During the process, the thicknesses of the oxide formed on the top (100) and sidewalls (110) surfaces are plotted in Fig. 5 for various fin widths. Fig. 6 shows the SEM image of a FinFET with condensed SiGe S/D after oxide removal. A TEM image of the gate stack is shown in Fig. 7. The physical gate length obtained is 26 nm.

Fig. 8 compares the I_D-V_G characteristics of a FinFET with SiGe S/D (uncondensed) and a control FinFET. Similar subthreshold swing and drain-induced barrier lowering (DIBL) are observed for the two devices. For a given gate-overdrive, the FinFET with SiGe S/D gives a higher drain current which can be mostly attributed to a reduction in series resistance. Fig. 9 plots the I_D-V_G characteristics of a FinFET with a condensed SiGe S/D and a FinFET with an uncondensed SiGe S/D. The L_G = 26 nm FinFET with condensed SiGe S/D shows a subthreshold swing of ~100 mV/decade and DIBL of 0.13 V/V. The I_D-V_D characteristics of the devices are plotted in Fig. 10 at various gate overdrives. At (V_G - V_t) of -1.2 V, the FinFET with condensed SiGe S/D shows a 28% higher I_{Dsat} than the FinFET with uncondensed SiGe S/D. This is possibly attributed to a recessed Ge profile and an increased Ge concentration for larger strain effects. The two devices have comparable source/drain series resistances, as deduced from a plot of the total channel resistance R_{tot} as a function of gate voltage (Fig. 11). At large $|V_G|$, R_{tot} exhibits asymptotic behavior and tends towards the source/drain series resistance. Fig. 12 plots the linear transconductance G_m as a function of gate overdrive for both SiGe S/D devices. The FinFET with condensed SiGe S/D shows a much higher peak G_m, than the FinFET with uncondensed SiGe S/D. The use of the Ge condensation process results in larger lateral compressive strain in the Si channel, leading to hole mobility enhancement that is manifested as a significant improvement in the transconductance.

CONCLUSION

P-channel FinFET with condensed SiGe S/D regions was demonstrated for the first time, with gate lengths down to 26 nm. 28% drive current enhancement was observed in comparison with a FinFET with an uncondensed SiGe S/D. The Ge condensation process is thought to lead to a more recessed Ge profile in the S/D regions and possible higher Ge concentration, both of which give rise to a higher uniaxial compressive strain for hole mobility enhancement. The Ge condensation process could be employed to enable further increase in Ge concentration for extreme strain scaling using source/drain stressors in aggressively scaled transistors.

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REFERENCES

[1] T. Ghani *et al.*, *IEDM Tech. Dig.*, pp. 978, 2003.
[2] P. Verheyen *et.al.*, *Symp. VLSI Tech.*, pp. 194-195, 2005.
[3] K.-J. Chui *et.al.*, *IEDM Tech. Dig.*, pp. 499-502, 2005.
[4] T. Tezuka *et al.*, *Appl. Phys. Lett.* 79, pp. 1798, 2001.

- V_t Adjust Implant
- Fin Patterning (W_{fin} = 30 nm)
- Sacrificial Oxidation
- Gate Oxidation ~ 3 nm
- Poly Si Gate Deposition, Definition.
- Spacer Formation

Removal of nitride stringer

- **Selective SiGe Epitaxy on Fin and S/D**
- **Ge Condensation: 950°C, 5 min**

- Hard Mask Removal
- S/D and Gate Implant.
- Anneal at 900°C

Fig. 1. Process flow for the fabrication of FinFETs with SiGe S/D formed by Ge condensation.

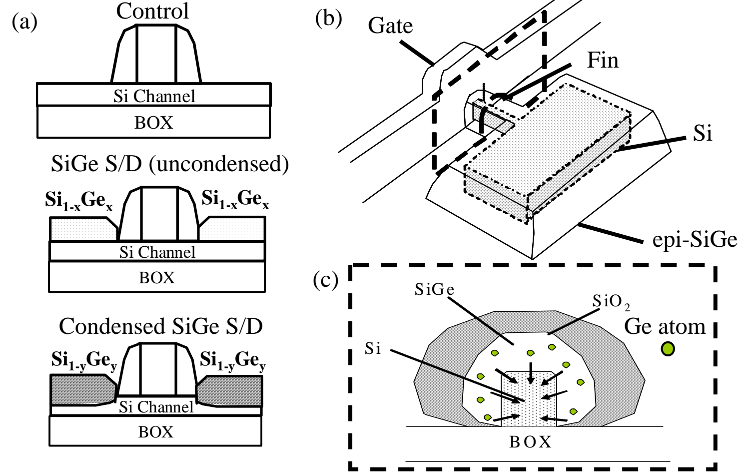

Fig. 2. (a) Device structures fabricated in this work. (b) Schematic showing the selectively grown SiGe on the fin and S/D regions. (c) A cross-sectional view of Ge condensation process at the fin. The oxidation of SiGe drives Ge atoms into the fin.

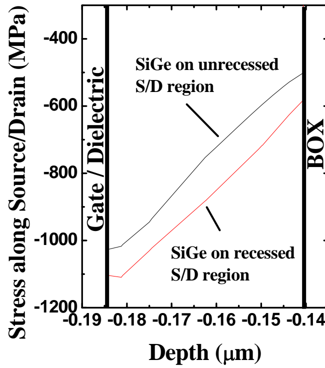

Fig. 3. Stress simulation for FinFET (fin width = 20 nm) with recessed profile shows a larger compressive strain.

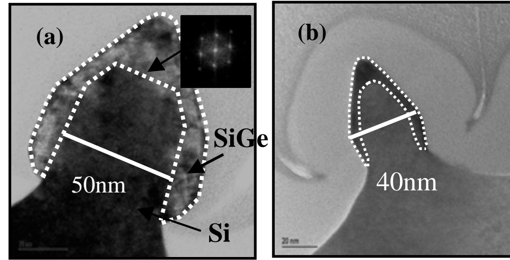

Fig. 4. (a) TEM image of a fin structure with SiGe grown on the top (100) and the sidewall (110) surfaces. (b) Ge diffuses into the fin after condensation at 950°C for 20 mins in an oxygen ambient.

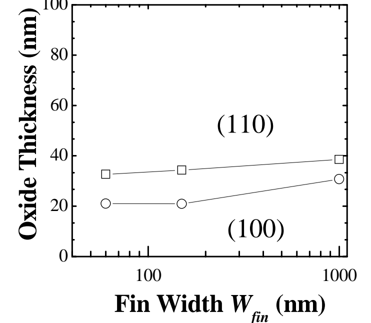

Fig. 5. Comparison of SiGe oxidation on (110) and (100) surfaces, i.e. the fin sidewalls and top surfaces, respectively.

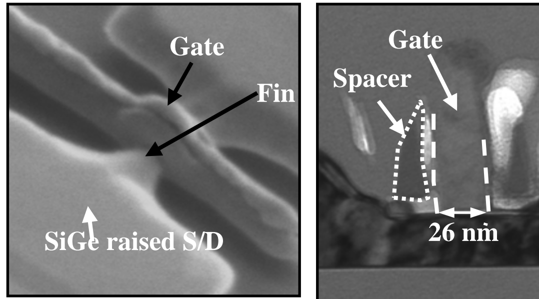

Fig. 6. SEM image of FinFET with SiGe S/D after condensation and oxide removal.

Fig. 7. TEM image of the gate stack, showing a gate length of 26 nm.

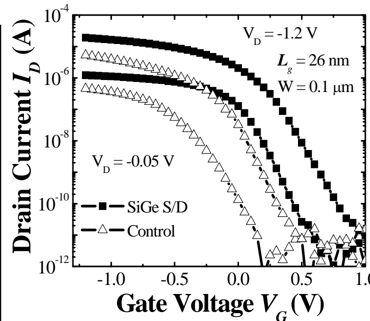

Fig. 8. Similar subthreshold characteristics observed for control device and FinFET with uncondensed SiGe S/D.

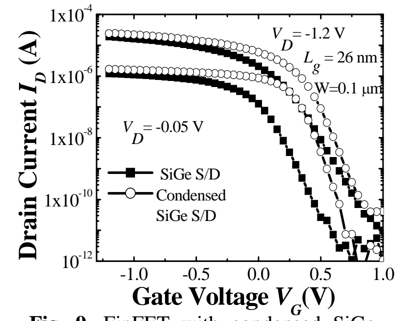

Fig. 9. FinFET with condensed SiGe S/D device shows better subthreshold characteristics.

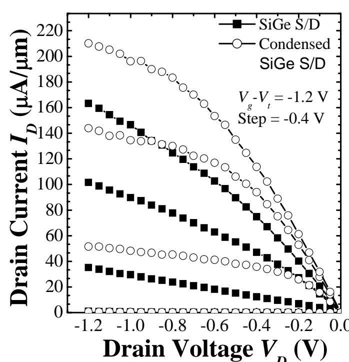

Fig. 10. I_D-V_D characteristics of FinFET devices at various gate overdrives (V_g-V_t). FinFET with condensed SiGe S/D shows a higher drive current.

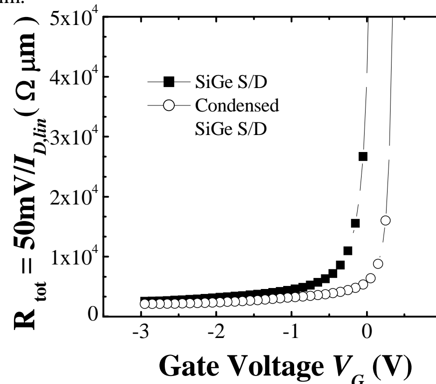

Fig. 11. Extraction of series resistance by examining the asymptotic behavior of the total resistance at large gate bias.

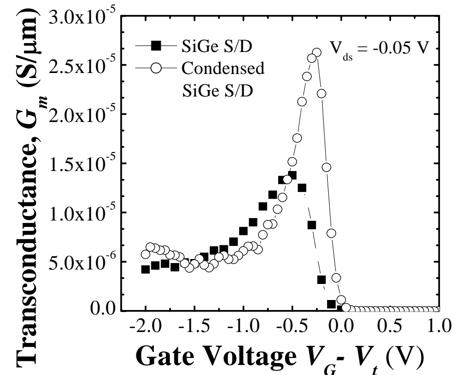

Fig. 12. Comparison of transconductance G_m at the same gate overdrive, illustrating an enhancement of 91% for the FinFET with condensed SiGe S/D over the FinFET with uncondensed SiGe S/D device.