

## Evaluating Strained/Relaxed-Ge, Strained-Si, Strained-SiGe For Future Nanoscale p-MOSFETs

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### Abstract

For the first time, the tradeoffs between short-channel (15nm) drive current ( $I_{on}$ ), intrinsic delay ( $\tau$ ), off-state band-to-band tunneling (BTBT) leakage and long-channel mobility ( $\mu$ ) have been systematically compared in futuristic high mobility channel materials, like strained-Si (0-100%), strained-SiGe (0-100%) and Ge. All possible combinations of strained  $Si_{(1-x)}Ge_{(x)}$  alloys grown on relaxed  $Si_{(1-y)}Ge_{(y)}$  virtual substrates have been evaluated. The optimal channel materials for nanoscale p-MOSFETs are discussed through detailed Full-Band Monte-Carlo, BTBT (including band structure and quantum effects), and 1-D Poisson-Schrodinger simulations on ultra-thin ( $T_s=5nm$ ), nano-scale ( $L_g=15nm$ ) DG FETs.

### Introduction

High mobility channel materials like strained-Si, Ge and strained  $Si_xGe_{1-x}$  are very promising as future channel materials [1]-[8]. Currently, strained-Si is the dominant technology for high performance p-MOSFETs and increasing the strain provides a viable solution to scaling. However, looking into future nanoscale p-MOSFETs, it becomes important to look at novel higher mobility channel materials, like Ge, strained-SiGe or strained-Ge, which may perform better than even very highly strained-Si. Most high mobility materials have a significantly smaller bandgap compared to Si and suffer from higher BTBT leakage, which can ultimately limit their scalability. Further, as we scale MOSFETs down to very short channel lengths, the relation between the long-channel mobility and short-channel drive current is not direct or obvious. In this work, through detailed BTBT (including band structure and quantum effects), Full-Band Monte-Carlo and 1-D Poisson-Schrodinger simulations on ultra-thin, nanoscale DG FETs, we systematically compare different high mobility channel materials in terms of the drive current, intrinsic delay and off-state leakage.

### Device Structures And Channel Materials

A common terminology used in this paper is a channel material (x,y) where, x denotes the Ge content in the channel material and y denotes the Ge content in an imaginary relaxed (r) substrate to which the channel is strained (s). E.g. (0.3,0) is a s-SiGe (with 30% Ge content) channel strained to an underlying Si substrate. (0,0.6) is a s-Si channel strained to a r-SiGe (60% Ge content) substrate. In this work, we have looked at all possible strained  $Si_{(1-x)}Ge_{(x)}$  alloys grown on relaxed  $Si_{(1-y)}Ge_{(y)}$  substrates. Four extreme cases are considered:

- 1) The biaxial tensile strained-Si on relaxed SiGe was varied from (0,0) r-Si to (0,1) s-Si.
- 2) The compressive strained-SiGe on relaxed Si was varied from (0,0) r-Si to (1,0) s-Ge.
- 3) The tensile strained-SiGe on relaxed Ge was varied from (0,1) s-Si to (1,1) r-Ge.
- 4) The compressive strained-Ge on relaxed SiGe was varied from (1,0) s-Ge to (1,1) r-Ge.

Fig. 1 shows the schematic of the device structure, device dimensions and channel materials that are investigated. The bandgaps ( $E_g$ ), ladders and effective masses used in this work are taken from [9]-[10] and are tabulated in Table 1.

### Transport: Long Channel Mobility / $I_{on}$ In Nanoscale FETs

Fig. 2 shows the calculated in-plane mobility for the different materials as function of strain due to the increasing Ge concentration in the SiGe layer. The mobility dramatically increases with increasing strain and increasing Ge concentration in

the layer because of a reduction in the conductivity mass and the band splitting due to strain. In extremely scaled MOSFETs, the relation between the short-channel drive current ( $I_{on}$ ) and the long-channel mobility ( $\mu$ ) is not direct or obvious. In order to accurately capture and understand the transport in nanoscale devices, Full-Band Monte-Carlo simulations were performed. The results for the drive current enhancement of the different high-mobility materials are plotted in Fig. 3. The highest drive currents are obtained from the compressive s-Ge on r-SiGe substrates, and for s-SiGe channels with very high (>0.8) germanium content grown on r-Si substrates.

### Performance: Intrinsic Delay

Due to its higher dielectric constant ( $\kappa_s$ ), Ge shows worse SCE compared to Si. Further, the lower effective mass in high mobility channel materials leads to a lower Density Of States (DOS) capacitance. This may lead to a reduction in the drive current but may not adversely affect the intrinsic delay of the device, which is determined by  $CV/I$ . Fig. 4 shows the intrinsic delay of the different devices. The lowest delays are obtained from the compressive s-Ge on r-SiGe substrates, and for s-SiGe channels with very high (>0.8) germanium content grown on r-Si substrates. Further, for s-Ge grown on r-SiGe, the intrinsic delay remains low and does not change significantly even as we increase the strain.

### Off-state Leakage: Band To Band Tunneling (BTBT)

Fig. 5 shows a typical  $I_d$ - $V_g$  characteristic of a p-MOSFET. The minimum achievable standby leakage ( $I_{off,min}$ ) is at the intersection of the BTBT leakage with the subthreshold leakage. Most high-mobility materials have a small bandgap and suffer from excessive BTBT leakage, which can ultimately limit their scalability. To accurately estimate  $I_{off,min}$  for different materials, we performed detailed BTBT simulations, which take into account bandstructure information, quantum mechanical (QM) effects and the direct-indirect valley transitions. Fig. 6, plots the  $I_{off,min}$  for the different (s/r)-SiGe alloys. The leakage current for s-Si on r-SiGe and s-SiGe on r-Si increases monotonically with increasing strain and increasing Ge content due to the rapid reduction in the  $E_g$  and the transport effective mass. The dependence of the off-state leakage for s-Ge on r-SiGe and s-SiGe on r-Ge is not monotonic and reveals an optimum point of minimum leakage. As we go from either (1,0) s-Ge or (0,1) s-Si to (1,1) r-Ge, the bandgap increases. However, (1,1) r-Ge shows higher leakage than (1,0) s-Ge due to the low-lying  $\Gamma$ -valley, which allows for a large direct BTBT leakage component. (0,1) s-Si has the highest  $I_{off,min}$  because of an extremely small  $E_g$ . The competition between the decreasing bandgap and the effect of the low-lying  $\Gamma$ -valley leads to an optimum minimum off-state leakage point.

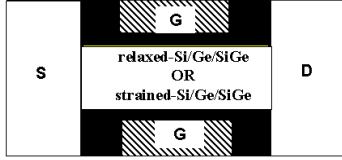
### Benchmarking The Different Materials: Power-Performance

A plot of the switching frequency ( $f_T$ ) vs. the minimum standby leakage ( $I_{off,min}$ ) achievable is a good benchmark to compare different device structures and channel materials. Fig. 7 benchmarks the performance of the different (s/r)-SiGe alloys. The x-axis ( $I_{off,min}$ ) determines if a given material can meet an off-state leakage specification, while the y-axis ( $f_T$ ) compares the performance of the materials that can meet the leakage requirements. We find that for higher Ge content (>60%), s-SiGe on r-Si performs much better than s-Si on r-SiGe. The highest performance is obtained in s-Ge (>2X enhancement compared to r-Si) on r-SiGe MOSFETs. We find that applying biaxial compressive strain to Ge increases its performance while simultaneously lowering the leakage. The optimum leakage point is

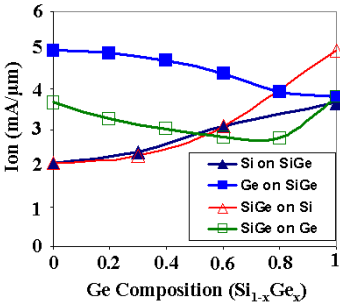
obtained for (1,0.6) s-Ge (>10X reduction compared to r-Ge). Fig. 8 shows the relative performance of (1,0.6) s-Ge compared to (0,0) r-Si, (0,1) s-Si, (1,1) r-Ge, (1,0) s-Ge.

### Conclusion

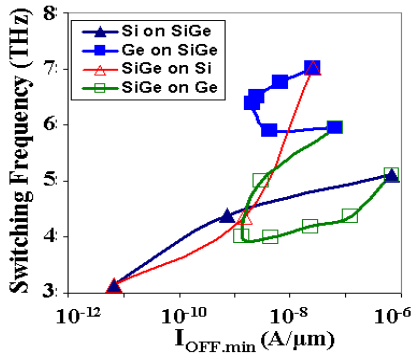
The optimal channel materials for future nanoscale p-MOSFETs are obtained through detailed BTBT (including band structure and quantum effects), Full-Band Monte-Carlo and 1-D Poisson-Schrodinger Simulations on ultra-thin (5nm), nano-scale (15nm) DG MOSFETs. The tradeoffs between drive current ( $I_{on}$ ), intrinsic delay ( $\tau$ ), band-to-band tunneling (BTBT) leakage and long-channel mobility ( $\mu$ ) have been systematically compared in futuristic high mobility channel materials, like strained-Si (0-100%), strained-SiGe (0-100%) and relaxed-Ge. Our results show that (x,0) strained-SiGe becomes the material of choice compared to (0,x) strained-Si for  $x>0.6$ . The highest performance is obtained in compressively strained-Ge MOSFETs (>2X enhancement compared to r-Si). Applying biaxial compressive strain to Ge increases its performance while simultaneously lowering the leakage. The optimum leakage point is obtained for (1,0.6) s-Ge (>10X reduction compared to r-Ge).



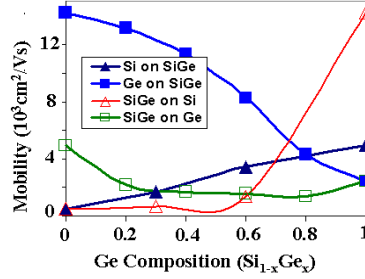
**Fig1:** DG FET different channel materials  $L_g=15\text{nm}$ ,  $T_s=5\text{nm}$ ,  $V_{dd}=0.7\text{V}$



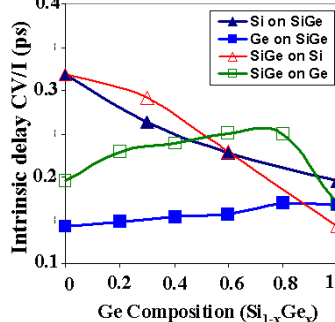
**Fig3:** Full-band Monte Carlo Drive current for the various channel materials. s-Ge on r-SiGe and s-SiGe on r-Si (for  $x>0.8$ ) exhibit the highest drive currents.



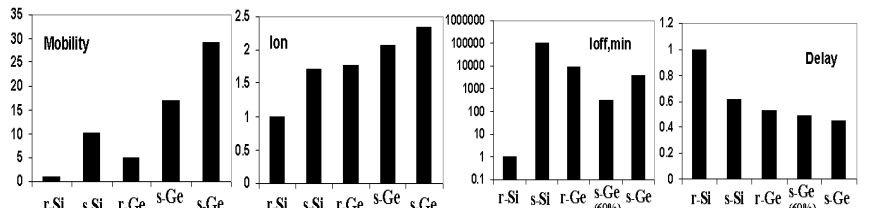
**Fig7:**  $f_T$  vs  $I_{OFF,MIN}$  for the various channel materials. (1,0.6) s-Ge shows an optimum reduction (>10X) in off-state leakage compared to (1,1) r-Ge and simultaneously achieving higher switching frequencies.



**Fig2:** In-plane mobility for the various channel materials. Mobility dramatically increases with increasing strain and Ge concentration.



**Fig4:** Intrinsic delay for the various channel materials. s-Ge on r-SiGe and s-SiGe on r-Si (for  $x>0.8$ ) exhibit the highest performance.



**Fig8:** Comparing the relative performance (with r-Si as reference) of compressive biaxially strained (1,0.6) s-Ge to (0,0) r-Si, (0,1) s-Si, (1,1) r-Ge and (1,0) s-Ge.

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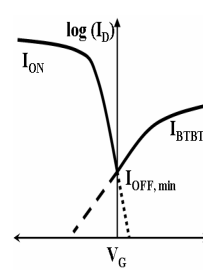
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### Acknowledgements

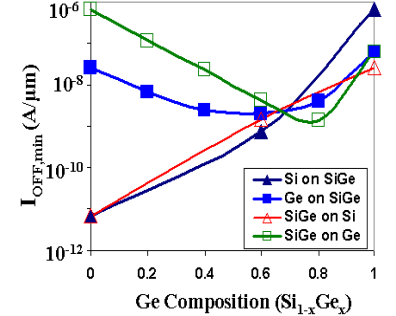
This work was sponsored by MARCO Materials, Structures and Devices Focus Center (MSD), Initiative for Nanoscale Materials and Processes (INMP) and an Intel Fellowship. The authors thank Mark Bohr, Tahir Ghani, Ken Uchida and Jeff Welser for useful discussions.

	Eg	Band	Ladder	$\Delta E$	mx	my	mz	g	offset
Si Relaxed <001>	1.12	Ec	$X_2$	0	0.19	0.19	0.92	2	0
			$X_4$	0	0.19	0.92	0.19	2	0
		Ev	$V_1$	0		0.49		1	0
			$V_2$	0		0.16		1	0
Ge relaxed <110>	0.66	Ec	$L_2$	0	0.08	0.573	0.218	2	0.05
			$L_2$	0	0.218	0.117	0.08	2	0.05
			$\Gamma$	0.14	0.038	0.038	0.038	2	0.19
		Ev	$V_1$	0		0.33		1	0.51
			$V_2$	0		0.043		1	0.51
			$\Delta_{001}$	0	0.19	0.19	1.04	2	-0.577
Strained Si 100% [001] Stress	0.39	Ec	$\Delta_{100}$	0.862	1.05	0.38	0.19	2	0.285
			$\Delta_{100}$	0.862	0.38	1.05	0.19	2	0.285
			$V_1$	0		0.51		1	0.153
		Ev	$V_2$	0.22		0.26		1	-0.067
			$V_3$	0.26		0.187		1	-0.107
			$\Delta_{100}$	0	0.19	0.98	0.19	2	0.135
Strained Ge 100% on <001> Si	0.498	Ec	$\Delta_{100}$	0	0.98	0.19	0.19	2	0.135
			$\Delta_{001}$	0.683	0.19	0.19	0.98	2	0.818
			$V_1$	0		0.125		1	0.821
		Ev	$V_2$	0.166		0.079		1	0.656

**Table1:** Material parameters for (0,1) s-Si, (1,0) s-Ge, (0,0) r-Si and (1,1) r-Ge, used in this study



**Fig5:**  $I_{OFF, min}$  is the minimum achievable leakage current in a MOSFET.



**Fig6:**  $I_{OFF,MIN}$  for the various channel materials. s-Ge shows a dramatic reduction in off-state leakage compared to r-Ge because of the lower leakage from the  $\Gamma$ -valley.