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Novel Elevated Source/Drain Technology for FinFET
Overcoming Agglomeration and Facet Problems Utilizing Solid Phase Epitaxy

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Abstract

For the first time, a novel low thermal-budget *S*olid *P*hase *E*pitaxy and selective *E*tching technology (SPE^2) for elevated *S*ource/*D*rain (S/D) structure was adapted to FinFET. Agglomeration and facet problems, which were inevitable by the conventional *V*apor *P*hase *E*pitaxy (VPE), were successfully solved.

1. Introduction

FinFET is one of the candidates for the double gate mode operated CMOS device, which realizes better cut-off characteristics and scalability than the planer mode operated CMOS [1]. Though, Okano et. al. reported that FinFET has not been obtained expectedly high current drive because of it's parasitic resistance [2]. They suggested the use of elevated S/D technology to reduce the parasitic resistance, but there are few reports on the elevated S/D for FinFET because of it's difficulties.

2. The Difficulty of Elevated S/D for FinFET

The *S*elective *E*pitaxial *G*rowth (SEG) technique by the vapor phase epitaxy has been widely adapted to the planar CMOS to form elevated structure and been achieved great successes to date [3,4].

Nevertheless, ordinal VPE has been revealed not to be adaptable to the elevated S/D for FinFET. The main issues are the agglomeration and the faceting of the Fin structure. Figure 1 shows the cross-sectional SEM images of the Fin structure before and after VPE. The narrow Fin structure made of single-crystalline Si was easy to agglomerate and could not sustain Fin shape under a typical 800˚C VPE condition. Figure 2 shows the faceting of the Fin after VPE. Fin is surrounded by the {110} facets, where wider Fin is selected to avoid an agglomeration. In the case of planar MOSFET, the optimized gate sidewall realized facet-free elevated structure [5]. In the case of FinFET, however, such a structural optimization of the edges of Fin is difficult because processes become too complicated to fabricate.

3. The Adaptation of SPE^2 to FinFET

3-1. Concept and Result:

In order to overcome these problems, we adapted SPE^2 technology to FinFET for the first time.

Figure 3 schematically illustrates SPE^2 process sequence for elevated S/D of FinFET. Firstly, amorphous Si (a-Si) is conformally deposited at 600˚C. Only the a-Si on the Fin S/D is epitaxially grown to single crystalline by solid phase epitaxy below 650˚C. Then the Si region which was not transformed to single-crystalline is selectively etched with HC1 vapor continuously in the same chamber below 650˚C. Low process temperature through these steps benefits to avoid agglomeration of Fin structure. Facet is also expected to be avoidable by this technology because the surface of elevated S/D is determined by the surface of deposited a-Si.

Figure 4 (a) shows TEM image of partially crystalline Fin structure just after SPE annealing at 600˚C for 900sec (step3). The deposited a-Si is transformed to the single-crystalline Si only on the Fin, while remaining amorphous on the dielectrics. And after selective etching, facet-free elevated S/D structure was successfully obtained as shown in fig. 4 (b) without agglomeration.

3-2. Suppression of Selective Deposition of a-Si:

In an early stage of experiments, we found out unintentional selective deposition of a-Si. Figure 5 (a) shows an example of selective deposition in which a-Si is not deposited on Fin (Si) and deposited on STI and SiN cap. To clarify the mechanism, we investigated selectivity under various a-Si deposition conditions varying growth rate. Experiments were performed at the constant temperature to obtain constant SPE rate for all the samples. Growth rate was controlled independently by changing partial pressure of the precursor. Figure 6 shows the relationship among growth rate, SPE rate and selectivity. It is clearly demonstrated that when growth rate is higher than SPE rate, a-Si is conformally deposited (fig. 5 (b)) and vice versa. Therefore, for the purpose of elevated S/D, we must choose a former condition.

4. Impact on the Device Performance

Figure 7 (a) shows the typical I_d-V_g characteristics for the CMOS-FinFETs with elevated S/D formed by SPE^2. Gate length (L_g) =20nm, fin width (W_{fin}) = 20nm, fin height (H_{fin}) = 50nm, and EOT=1.3nm. The drain currents are normalized by channel width ($W_{channel}$), where $W_{channel}$ is defined as $2\times H_{fin}$. Plan view SEM image of FinFET by SPE^2 is also shown in fig.7 (b). Current drivability is shown to be remarkably improved by the effect of elevated S/D as shown in fig. 8.

5. Conclusions

As an technique to form elevated S/D, SPE^2 was adapted to FinFET for the first time. Fin agglomeration and facet issues were successfully settled. By the reduction of parasitic resistance, current drivability was dramatically improved. SPE^2 is a fitting method for elevated S/D of FinFET.

References

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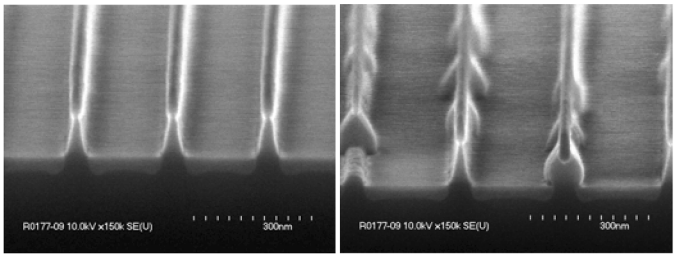


(a) before VPE (b) after VPE

Fig. 1 SEM images of the Fin structure before and after VPE. VPE : 800˚C, 40Torr, $SiH_2Cl_2/HCl/H_2$ gas mixture

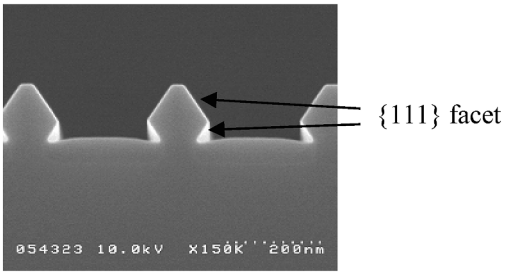


Fig.2 SEM images of the Fin structure surrounded with {111} facets.
VPE condition is the same as figure1.

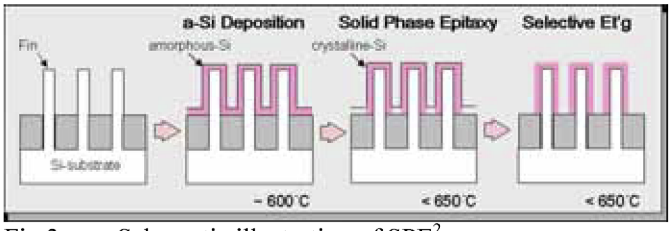


Fig.3 Schematic illustration of SPE^2 process sequence. Process temperature is maintained below 650˚C through the sequence.

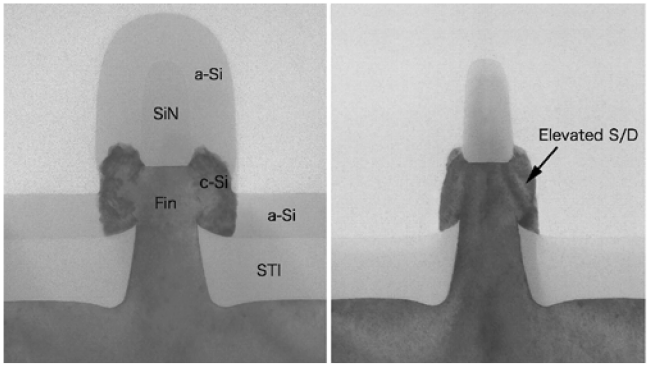
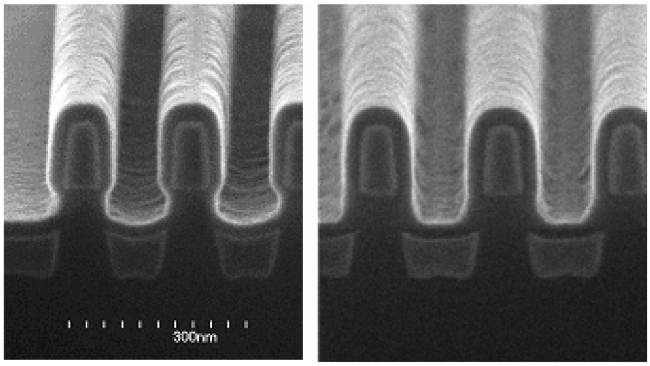


Fig. 4 Cross-sectional TEM image of Fin structure after solid phase epitaxy and selective etching.



(a) Selective deposition (b) Conformal deposition

Fig. 5 Selective and conformal a-Si deposition on Fin structure. Only partial pressure of SiH_4 is varied under constant temperature of 600˚C.

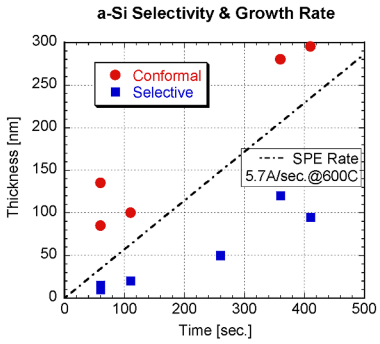
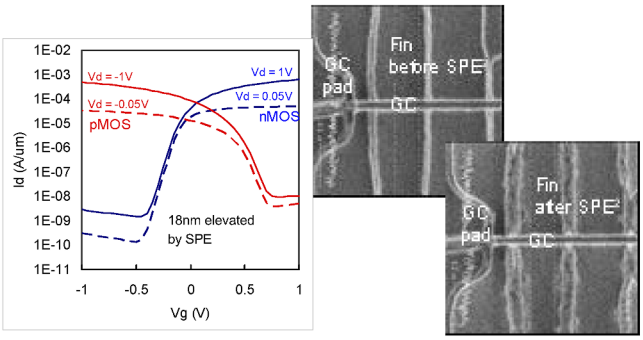


Fig. 6 The relationship between growth rate of a-Si, SPE rate, and selectivity. Selective when growth rate is higher than SPE rate. Conformal when growth rate is lower than SPE rate.



(a) Id-Vg characteristics (b) Plane view image of Fin transistor

Fig. 7 (a) I_d-V_g characteristics of FinFET and (b) plan view image of transistor before and after SPE^2. L_g = 20nm, W_{fin} = 20nm. Drain currents are normalized by $W_{channel} = 2 \times H_{fin}$.

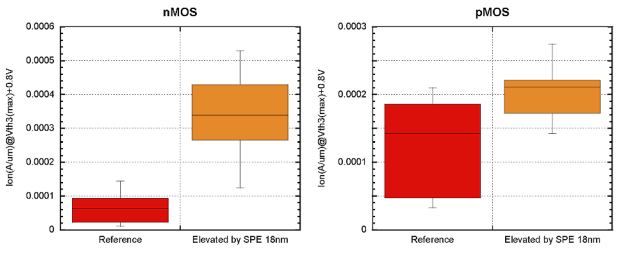


Fig. 8 I_d improvement with elevated S/D by SPE^2. Improvements were about 400% and 150% for nMOS and pMOS respectively.