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Novel Gate-All-Around MOSFETs with Self-Aligned Structure

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1. Introduction

The gate-all-around (GAA) MOSFETs are ideal device structures in CMOS scaling. In the GAA device, the channel region is surrounded by the gate electrode. Therefore, it provides robust short-channel effect (SCE) immunity, high driving current, and excellent transconductance characteristics [1][2]. However, complicated process is required to fabricate the GAA MOSFETs. Moreover, with conventional processes, it is not easy to form the complete self-aligned gates. In the multiple gate MOSFETs, it has been generally known that the gate misalignment induces the degradation of device performance [3].

In this paper, we present a novel self-aligned structure for GAA MOSFETs which needs only one mask to define all gates at the same time. Using the fabrication method of the 30-nm self-aligned FinFET with a large source/drain (S/D) region proposed by D. -S. Woo *et al*. [4], the self-aligned GAA MOSFETs can be fabricated by adding some processes. Since the wide S/D structure reduces the parasitic resistance, the current drivability can be considerably enhanced as compared with conventional FinFETs.

On the other hand, in the proposed self-aligned GAA MOSFETs, to make a cavity underneath a silicon channel, the buried oxide layer should be wet-etched. Due to the isotropic property of wet etching process, the bottom gate length is slightly oversized. We have already performed a simulation-based analysis on effects of the oversized bottom gate in self-aligned GAA MOSFETs [5]. In particular, for this device, the lateral S/D doping gradient should be small because the S/D junctions are formed by the prolonged diffusion of impurities. Therefore, it is expected that the oversized bottom gate leads to the enhancement of the gate controllability and the suppression of SCE.

2. Device Fabrication

The key process flow used in this work is schematically illustrated in Fig. 1. The starting material is p-type (100) SIMOX wafer. To thin the top silicon layer down to 48 nm, the initial oxide is grown and etched. An amorphous-Si/SiO_2 layer is stacked on the active region and dry-etched after the e-beam patterning to make the channel hardmask. A 40-nm TEOS sidewall spacer is formed before the S/D implantation. As^+ ions are implanted at energy of 20 keV and a dose of 1×10^{15} /cm^2 as shown in Fig. 1 a). For the groove formation, a 100-nm TEOS dummy layer is deposited and dry-etched after the e-beam lithography as show in Fig. 1 b). To make the silicon fin, the SOI is dry-etched across the channel hardmask and groove mask as shown in Fig. 1 c). The buried oxide layer underneath a silicon channel is removed by using wet etching and then the cavity is formed under the fin as shown in Fig. 1 d). A 5-nm sacrificial oxidation process is used to remove the damaged layer due to dry etching. After eliminating the sacrificial oxide, a 2.4-nm thick gate oxide is grown. A poly-silicon layer is deposited using LPCVD and doped with $POCl_3$. The gate is formed by the etchback process. The S/D doping profiles are diffused to the fin edge by a proper annealing process. Finally, back-end processes such as ILD deposition, photo-lithography for the contact, and aluminum metallization are performed.

Fig. 2 shows top view microscope images of a self-aligned GAA MOSFET. Fig. 3 shows the SEM image of the channel hardmask and the groove formation.

In this device, the gate length might be smaller than the groove width due to the oxide growth on (110) surfaces at the edge of the S/D during the gate oxidation. The fin width is reduced by the sacrificial and gate oxidation. Therefore, the minimal gate length and the fin width are evaluated at 35 and 20 nm, respectively.

3. Results and Discussion

Fig. 4 shows the I_d-V_g curve of the self-aligned GAA MOSFET with the 35-nm gate length and 20-nm fin width. The linear extrapolation method is used to extract the threshold voltage. Driving currents are normalized by the fin width, 20 nm. For this device, the threshold voltage, drain-induced barrier lowing (DIBL) and subthreshold slope (SS) are -272 mV, 79.0 mV/V and 45.2 mV/dec, respectively. The value of the threshold voltage appears impractical since we use the n^+ poly-silicon gate without channel doping. However, this problem can be rectified by using metal or metal silicide gates with an appropriate work function [6].

Transconductance characteristics are also shown in Fig. 4. The maximum transconductance of 690 mS/mm is obtained. We have confirmed that DIBL and SS are properly suppressed in spite of the short channel length.

Fig. 5 shows typical I_d-V_d characteristics for the fabricated device. The gate voltage is biased from 0 V to 1.0 V with 0.25 V step. Due to a large source/drain structure, driving current is high.

Fig. 6 shows DIBL as a function of the physical gate length for the self-aligned GAA MOSFETs. The fin width and the fin height are fixed at 30 and 48 nm, respectively. As the gate length increases, DIBL gradually decreases. DIBL is very well controlled and dose not exceed 50 mV. The very low DIBL demonstrates the advantage of GAA MOSFETs. The reason for less SCE is that the channel is tightly controlled by the surrounded gate electrodes.

4. Conclusion

Self-aligned GAA MOSFETs have been successfully fabricated. A complete self-aligned structure is implemented by using conventional CMOS processes. The devices also have wide S/D fan-out regions. Minimal gate length and fin width are 35 and 20 nm, respectively. The gate oxide thickness is 2.4 nm. The fabricated devices show the robust SCE immunity and the large current drivability.

Acknowledgement

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References

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a) Channel hardmask formation and source/drain implantation after SOI thinning.
b) Groove mask formation using TEOS deposition, e-beam lithography and dry etching
c) SOI etching across the channel hardmask and the groove mask to form the groove
d) Bottom oxide removal using dry and wet etching
e) Gate oxidation and n^+ poly-silicon gate formation

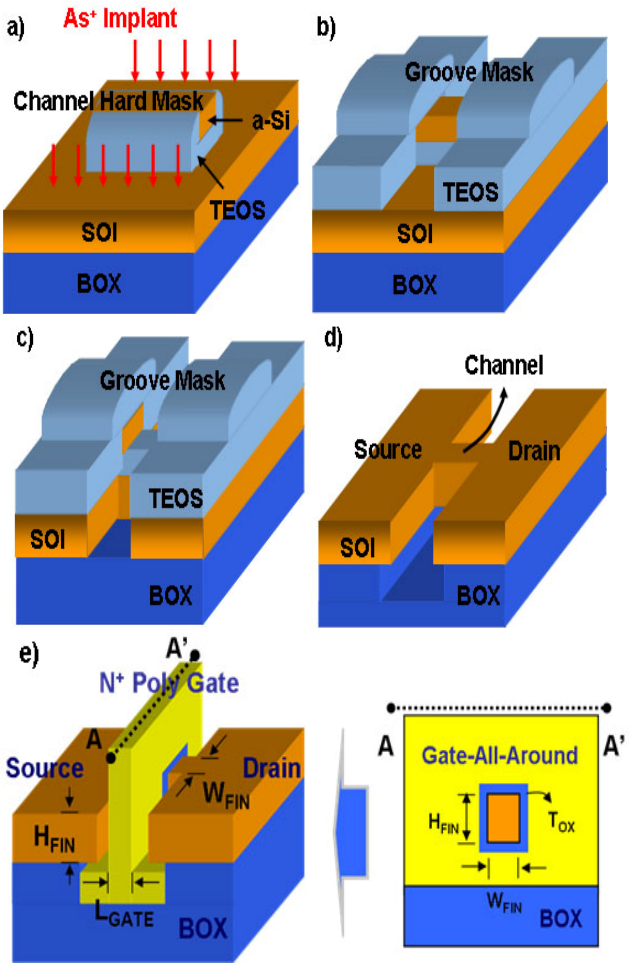

Fig. 1 Key process flow sequence and schematic diagram including the bird's eye view of the self-aligned GAA MOSFETs.

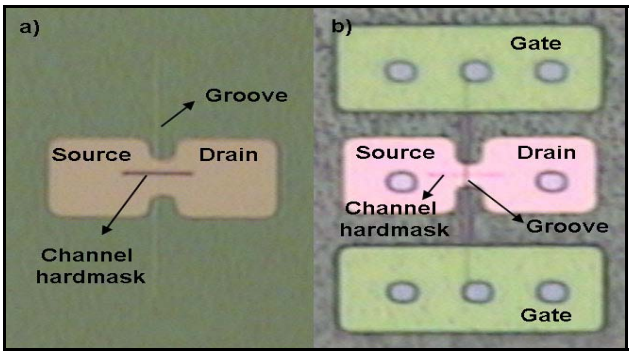

Fig. 2 Top view microscope images of the device a) after the groove formation and b) the photo-lithography for the contact.

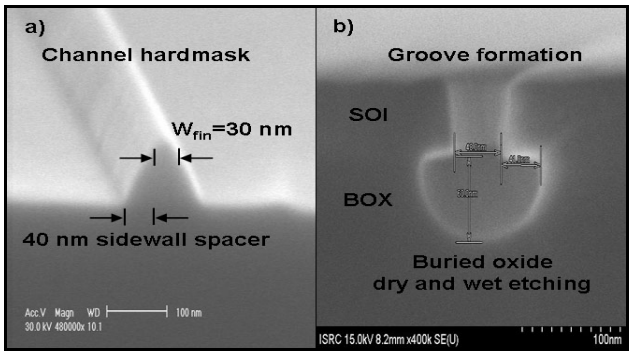

Fig. 3 SEM images of a) the channel hardmask and b) the groove region. Minimal groove width is 40 nm.

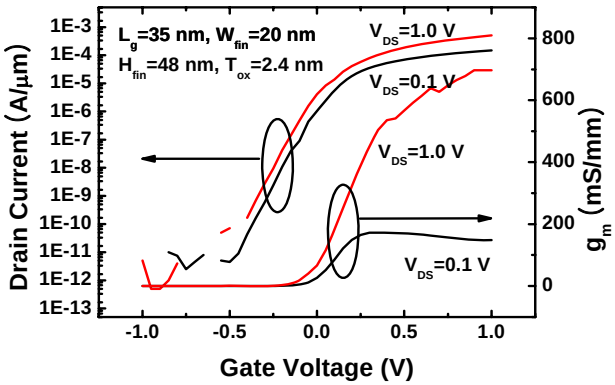

Fig. 4 I_d-V_g characteristics of a self-aligned GAA MOSFET. The gate length and the fin width are 35 and 20 nm, respectively.

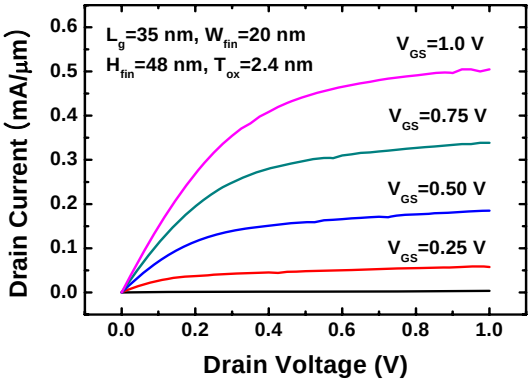

Fig. 5 I_d-V_d characteristics of the self-aligned GAA MOSFET. Due to the large source/drain structure, driving current is high.

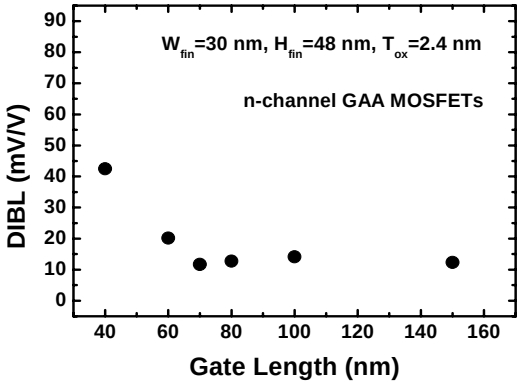

Fig. 6 DIBL as function of physical gate length for the fabricated self-aligned GAA MOSFETs.