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Improvement of Bulk CMOS Electrostatic Integrity using Germanium and Carbon co-implantation

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1. Introduction

In order to immunize CMOS bulk devices against Short Channel Effect, junction depth and lateral diffusion must be reduced in Source/Drain Extensions. Flash or Laser anneals can be performed to enhance dopant activation without diffusion but new tools are needed [1,2]. We present in this paper the impact of Germanium and Carbon implantation on Boron, BF_2, and Phosphorus diffusion through interstitial diffusion control that enables low junction depth down to 14 nm and low Short Channel Effect dependency devices without Ion/Ioff performances degradation.

2. CMOS devices integration

After STI block and well implantation, a nitrided oxide SiON with an EOT of 13Å was grown. After gate patterning down to 40nm, co-implantation was realized in Source/Drain Extension process step by 3 successive implantations with Germanium, Carbon and Boron or BF_2 for PMOS devices and Germanium, Carbon, Arsenic and/or Phosphorus for NMOS devices. Then process steps are standard with a dopant activation anneal achieved with a 1055°C spike RTP and nickel silicided contacts. Fig. 1 shows the impurities profiles for Germanium, Carbon and BF_2 in silicon substrate simulated with SRIM.

3. Electrical results and discussion

Germanium and carbon impact on Boron diffusion

It has already been shown that Germanium implantation added to Carbon implantation reduce Boron diffusion [3,4]. Germanium implantation reduces SCE thanks to the reduction of channeling with the Ge Pre-Amorphisation Implantation (PAI) and Ge+C+B co-implantation also improves SCE with a Carbon effect on Boron diffusion. Fig. 2 presents the saturated threshold voltage as a function of different gate length. Germanium and Carbon have a positive impact on SCE compared to Boron only but even with 0.5keV boron implantation energy in order to reduce junction depth SCE is worst for Ge+C+B split than for standard BF2 reference. Furthermore, the Ion/Ioff performances for Ge+B and Ge+C+B co-implantations compared to BF2 reference (Fig. 3) shows that PMOS devices are in punch-through regime for Lg = 40 nm due to too low threshold voltage values. Furthermore Boron implantation below 1 keV will hardly be an industrial solution due to non-uniformity of Boron beam at low implantation energy.

Germanium and carbon impact on BF2 diffusion

Fig. 4 shows an increasing improvement of SCE for Ge+BF_2 (channeling reduction with Ge PAI), C+BF_2 (Boron diffusion reduction with Carbon) and Ge+C+BF_2 (both effect). It is important to notice that BF_2 diffusion is also impacted with C implantation only whereas Boron is not. Fig.2 and Fig.4 show that Carbon implantations reduce Boron diffusion when the silicon crystal is amorphised with Germanium PAI or with BF_2 which is enough heavy to amorphise silicon whereas Carbon or Boron only are not. Fig. 5 shows that all co-implantations splits are on the same Ion/Ioff trend line for Lg = 40 nm. Fig. 6 sums up the reduction of SCE by Ge and/or C effects on B/BF_2 by showing the Drain Induced Barrier Lowering as a function of different gate lengths. MASTAR model is used to fit the V_{thsat}(L) curves (Fig.4). Tab.1 shows that junction depth is reduced to ~14nm and the lateral diffusion per side under the gate can be reduced by a factor of 4 with conventional implantation and anneal. Fig. 7 presents the Id(Vg) curves for all co-implantation splits. The sub-threshold voltage slope is improved from 115mV/dec for BF_2 to 97mV/dec for Ge+C+BF_2 co-implantation. Fig. 8 shows that lateral junction leakage is strongly degraded with Ge and/or C implantations due to an increased junction abruptness and to the introduction of defects in the junction depletion layer.

Germanium and carbon impact on Phosphorus diffusion

As Phosphorus diffusion is assisted by interstitial defects, it is expected to be slowed by Ge and/or C co-implantations. This is confirmed in Fig. 9 by the SCE reduction of Ge+C+P split compared to P only one. But devices are in punch-trought regime with Phosphorus only. The implantation of Arsenic As in the junction improves the SCE. Fig. 10 shows that As+P and Ge+C+As+P are on the same Ion/Ioff trend line for several gate length. Fig. 11 shows that the introduction of Phosphorus can decrease the lateral junction leakage thanks to the diminution of the junction abruptness.

4. Conclusion

We have demonstrated that Carbon implanted can reduce the Boron or Phosphorus diffusion in Source/Drain Extensions only if the silicon substrate is amorphised with a Germanium PAI or in a simpler way by the auto-amorphising specie BF_2. Carbon added to BF_2 in the Source/drain Extensions is an easy and low cost way to control Short Channel Effect for high performance devices.

Acknowledgement

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References

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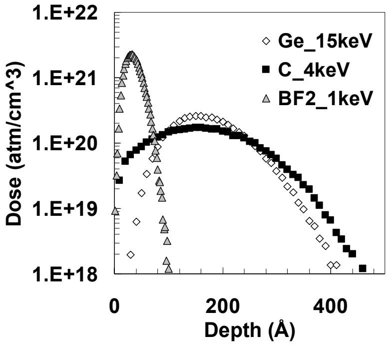

Fig.1: Impurities profiles simulated with SRIM for Germanium 15keV, Carbon 4keV and BF2 1keV.

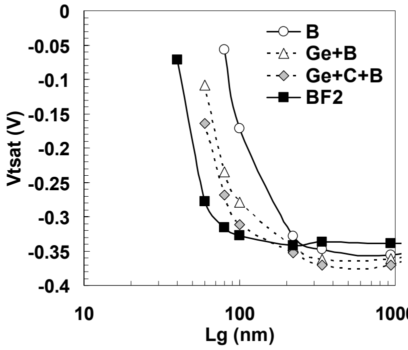

Fig.2: Threshold voltage as a function of different gate length for Germanium+Boron, Germanium+Carbon+Boron co-implantation and BF_2

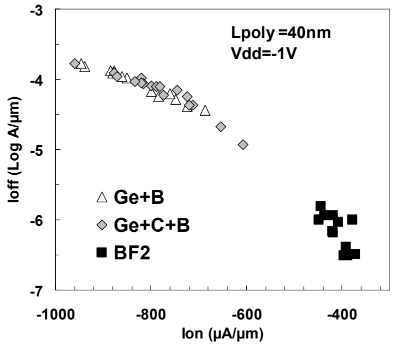

Fig.3: Ion/Ioff performances for Germanium+Boron, Germanium+Carbon+Boron co-implantation and BF_2

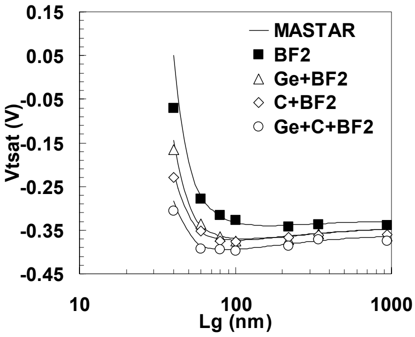

Fig.4: Threshold voltage for different gate length for BF_2, Ge+BF2, C+BF_2 and Ge+C+BF_2 co-implantation. Vth(L) can be fitted with MASTAR to extract junctions parameters.

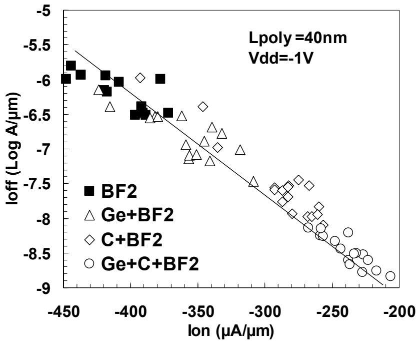

Fig.5: Ion/Ioff performances for BF_2, Carbon+ BF_2 and Germanium+BF_2 co-implantation

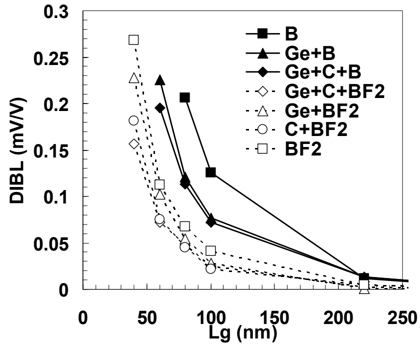

Fig.6: DIBL as a function of gate length for co-implantation with Boron or BF2

	BF2	Ge +BF2	C +BF2	Ge + C +BF2
Xj MAS-TAR (nm) ±3nm	22	20	17	14
Lateral Diffusion per side (nm) ± 3nm	5.5	4	2.5	1.4
Effective length Leff for Lg=45nm (nm)	34	37	40	42

Tab.1: Junction depth and lateral diffusion per side calculated with MASTAR model for BF2, Ge+BF2, C+BF2 and Ge+C+BF2 splits

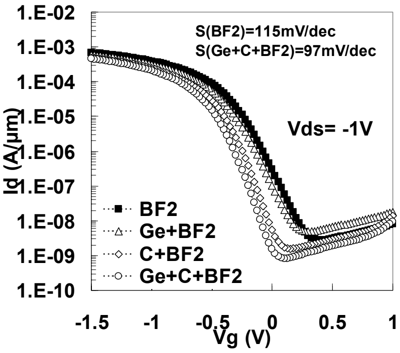

Fig.7: Id(Vg) curves for BF2, Ge+BF2, C+BF2 and Ge+C+BF2 splits. Sub-threshold voltage slopes are measured for BF2 and Ge+C+BF2

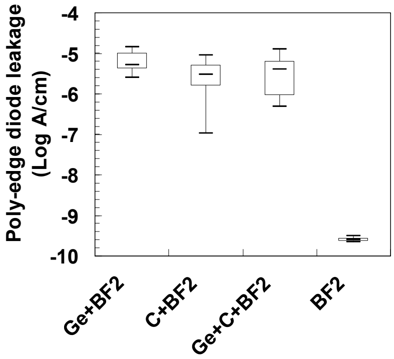

Fig.8: Lateral diode leakages induced by Source/Drain extensions for BF2, Ge+BF2, C+BF2 and Ge+C+BF2 splits

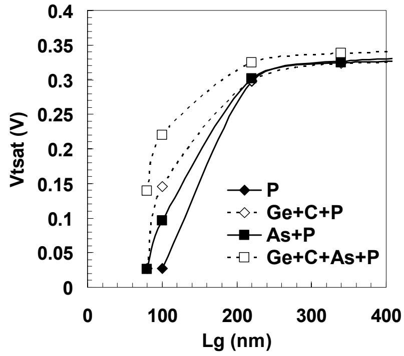

Fig.9: Threshold voltage as a function of different gate length for P, As+P and Ge+C+As+P co-implantation

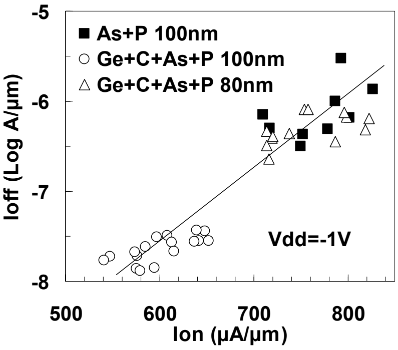

Fig.10: Ion/Ioff performances As+P and Ge-+C+As+P co-implantation splits for several gate length devices

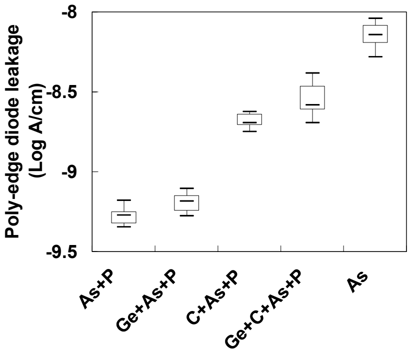

Fig.11: Lateral diode leakages induced by Source/Drain extensions for As+P, Ge+As+P, C+As+P, Ge+C+As+P and As splits