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Potential of and Issues with Multiple-Stressor Technology (MST) in High-Performance 45nm Generation Devices

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Abstract

In this paper, we describe multiple-stressor technology (MST) for high-performance 45-nm-node devices. The combination of two or more stressors, – poly-stressor/tensile stress liners (SL) for NFET, and embedded-SiGe/compressive-SL for PFET – is integrated and potential performance enhancement is investigated. Moreover, the issues of MST are also discussed from the viewpoint of variations in the device characteristics under extremely high channel stress, which have not been pronounced in the previous technology with its relatively low stress levels.

Introduction

As CMOS technologies are scaled into the sub-30nm regime, the simple scaling of gate length cannot be a candidate for enhancing circuit performance any more, because the rapid fall in drive current is much more dominant than the reduction in gate capacitance. In such a situation, process-induced uniaxial strain technology is indispensable for maintaining the roadmap target, and thus has been intensively investigated. Recently, in order to obtain further current-drive enhancement, multiple-stressor technology (MST) has been introduced, in which a combination of two or more strained silicon technologies is applied to strengthen the channel stress [1-5]. Indeed, excellent performance has been demonstrated with MST, however, issues in such a highly-stressed device have not been well-discussed. In this paper, focusing on MST, we explore its impact on scaled devices for the 45-nm technology node, and the resulting issues that become pronounced under extremely high stress levels are comprehensively investigated.

Multiple-Stressor Technology

As is well known, Piezoresistance (PR) coefficients are a good measure for estimating mobility enhancement as well as current-drive enhancement in strained silicon CMOSFETs without considering complicated phenomena such as subband splitting and band deformation. Table I summarizes experimental PR coefficients [6], and it is clear from this table that longitudinal tensile and vertical compressive strains for NFETs, and longitudinal compressive strain for PFETs are the most effective ways of enhancing the performance of <110> channel devices on an Si(001) surface. Taking this into account, Fig. 1 shows a schematic diagram of a suitable MST to obtain maximum CMOS performance enhancement. In addition to using a dual stress liner (SL) as a stopper during contact etching, a poly-stressor was used to enhance the vertical compressive stress in NFETs, and embedded-SiGe (e-SiGe) was adopted to achieve higher longitudinal compressive stress in PFETs.

Results and Discussion

Fig. 2(a) shows the process flow for integrating poly-stressor technology. Gate preamorphization was performed just before NSD implant, followed by the forming of a cap layer only in the NFET area. The PFET SD region was then etched for e-SiGe, using the capping layer as a hardmask following SiGe epitaxy, SD activation, and poly re-crystallization annealing. Finally, the capping layer was removed by wet etching for the Ni silicide module. Figure 2(b) shows a cross-sectional TEM of a poly-stressed NFET with tensile-SL. The dark contrast in the channel region exhibits the high vertical compressive stress and longitudinal tensile stress that were introduced into the channel by MST. The vertical and longitudinal strains in the channel (point 1 in Fig. 2(b)) were evaluated by nano-beam electron diffraction (NBD) and they are approximately 0.4 and -0.6%, respectively. Because the poly-stressor combined with SL has high compatibility with e-SiGe as a stressor for PFETs, and can easily introduce a relatively high stress, it is very promising for MST in NFETs.

With PFETs on the other hand, e-SiGe and compressive-SL can be easily integrated as MST, and are most effective in enhancing the performance as already mentioned. Figure 3 shows the gate length dependence on the PFET channel stress simulated by a 2-D process simulation [7]. By combining e-SiGe and compressive-SL, we were able to show that the resultant channel stress becomes simply additive both in the longitudinal and vertical directions. Figure 4 shows the result of MST for PFETs. From the I_{on} baseline with e-SiGe and tensile-SL (stressor for NFETs), 18% enhancement was achieved by applying compressive SL instead, and an excellent performance of I_{on} = 570 μA/μm at L_{min} (L_g@I_{off} = 100 nA/μm) = 32 nm was obtained. Figure 5 compares the gate length dependence on the effective hole mobility with and without MST extracted by the double-L_m method [8]. Compared with the single-stressor (Fig. 5(b)), MST shows a drastic increase in hole mobility with decreasing gate length (Fig. 5(a)), supporting the data shown in Fig. 4. This result indicates that compressive-SL only cannot introduce enough stress, and there still remains room to enhance the drive current by increasing the channel stress, especially for strong halo devices. Figure 6 shows the I_{on}-I_{off} characteristics as a function of the elevated SiGe-SD height for PFETs with MST. One of the key physical parameters in e-SiGe technology is the elevated-SD height, and it has been reported that higher elevated-SD results in a higher performance [9]. However, the reduction in effective gate height with increasing elevated-SD height is counteracted by the channel stress from SL [10]. In Fig. 6, I_{on} increases by 18% with increasing elevated-SD height from 0 to 25 nm even for MST PFETs, which suggests that stress from the e-SiGe is dominant in MST devices.

Although MST is very promising as a booster for the scaled device as shown previously, we have to consider some issues that arise in using this technology. Figure 7 shows the gate-width dependence on the PFET drive current for devices with and without MST. The combination of e-SiGe and compressive-SL degrades the performance of the narrow channel device severely (Fig. 7(b)) compared to a single-stressor device (Fig. 7(a)). This is because the SD region of the MST device is elevated; therefore, a transverse compressive stress from SL is effectively applied to the channel, leading to the degraded I_{on} as predicted by the PR coefficient in Table I. Furthermore, layout-dependent stress variation and its impact on the device characteristics are another issue. Figure 8 shows the simulated stress distribution of a 3-stacked layout (PFET). The important thing in this figure is that the poly-to-poly spaces in the dense pattern are completely filled with SL. In Fig. 8(b), it can be clearly seen that longitudinal stress in the device on the right out of the 3-stacked FETs is not symmetrical, and the average stress levels at the center, right, and isolated devices are quite different. The impact of this kind of stress distribution was confirmed by the actual device characteristics as shown in Figs. 9 and 10. Figure 9 shows the I_{on}-I_{off} characteristics of isolated and dense layout devices. In the case of a device highly-stressed by MST (Fig. 9(b)), the I_{on} degradation for the small poly-to-poly space, L_{pp}, that corresponds to the lower channel stress is remarkable in contrast to the negligible impact for the low-stressed device (Fig. 9(a)). Figure 10 depicts the correlation between the forward and reverse drive current as a function of the source-side diffusion length, L_s, measured by changing the source and drain terminals. The decrease in L_s means a decrease in the compressive stress from the stressors. If the stress level is relatively low, the forward and reverse currents are well-correlated and the impact of asymmetrical channel stress is almost negligible as shown in Fig. 10(a). However, when the device is highly-stressed, the higher channel stress near the drain-side compared to that on the source-side shows a superior performance (Fig. 10(b)).

Finally, Table II summarizes the potential of and issues with MST. In order to fully enjoy the potential high performance enhancement of this technology in the 45-nm generation and beyond, there still exists some issues to be solved.

Conclusions

We have investigated the impact of multiple-stressor technology, and demonstrated that the combination of two or more stressors brings additional performance enhancement. We have also clarified some issues, such as I_{on} degradation in the narrow-width region and variations in the layout-dependent characteristics as a consequence of channel stress variations when using MST. There is no doubt that MST is promising for further enhancing the drive current; in order to enjoy the high potential of MST in the 45-nm technology node, these issues must be taken into account.

References

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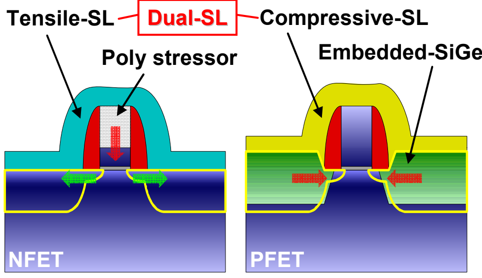
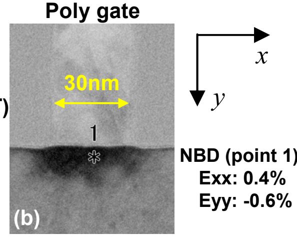


Fig.1 Schematic drawing of multiple-stressor technology to obtain maximum CMOS performance enhancement.



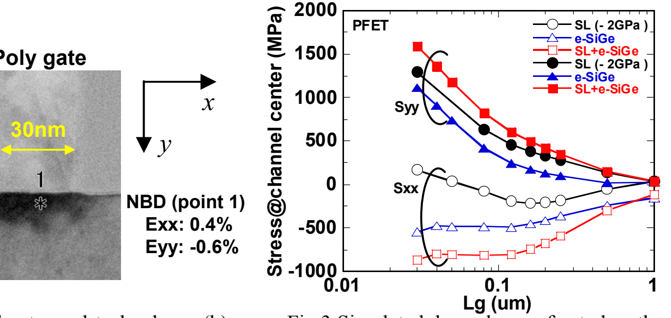


Fig.2 (a) Process flow of poly-stressed technology. (b) TEM cross-section of poly-stressed NFET with tensile SL. Channel strain was evaluated by NBD.

Fig.3 Simulated dependence of gate length on the PFET channel stress for single- and multiple-stressor devices.

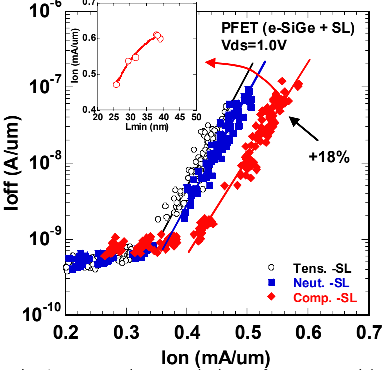


Fig.4 I_{on}-I_{off} characteristics of PFETs with e-SiGe for different kind of SLs. Inset shows the I_{on}-L_{min} tradeoff of the device with compressive-SL over e-SiGe.

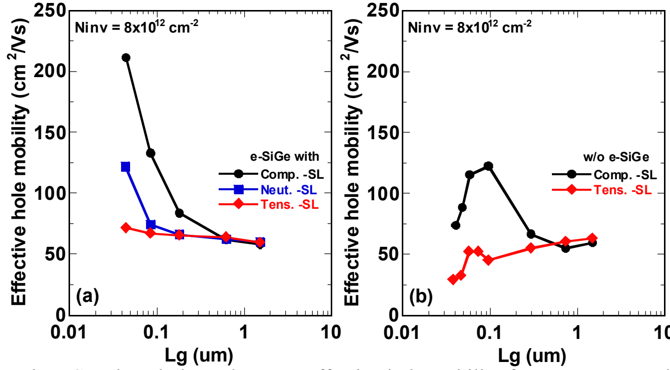


Fig.5 Gate length dependence on effective hole mobility for PFETs stressed by (a) multiple-stressors (e-SiGe and SL) and (b) single-stressor (SL only).

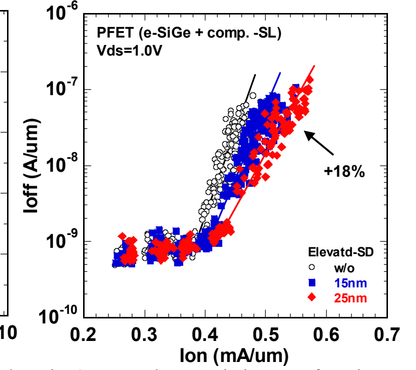


Fig.6 I_{on}-I_{off} characteristics as a function of elevated SiGe-SD height for PFETs stressed by e-SiGe combined with compressive-SL.

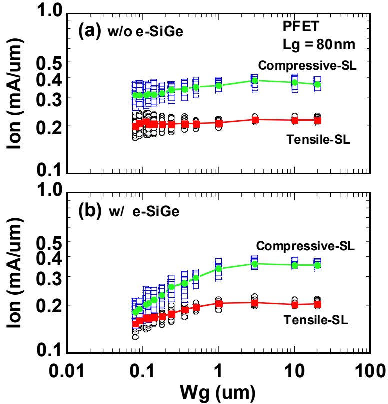


Fig.7 Gate width dependence on PFET drive current for the devices (a) without e-SiGe and (b) with e-SiGe.

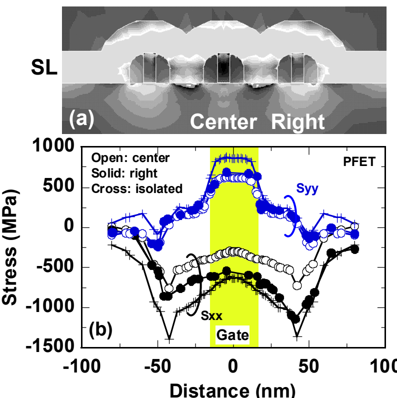


Fig.8 Simulated stress distribution of 3-stacked layout. (a) 2D horizontal stress (S_{xx}) distribution in which white corresponds to compressive, (b) 1D-cut along the channel for the center, right, and isolated devices.

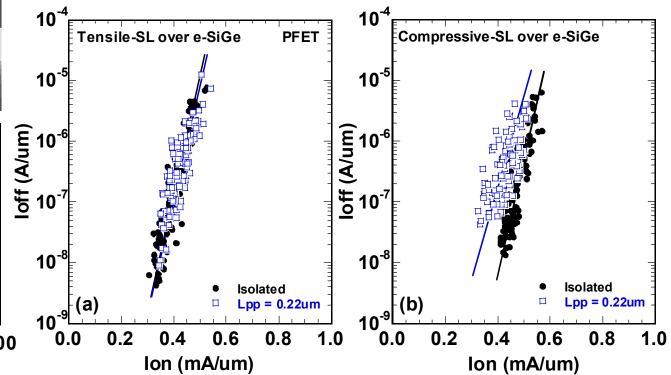


Fig.9 I_{on}-I_{off} characteristics of isolated and dense layout devices. (a) PFETs with tensile-SL over e-SiGe, (b) PFET with compressive-SL over e-SiGe. Poly-to-poly space (L_{pp}) for dense layout is 0.22μm.

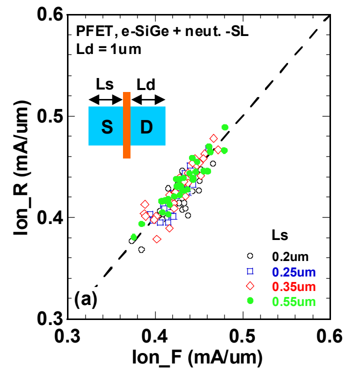


Fig.10 Correlation between forward and reverse drive current as a function of source-side diffusion length (L_s) measured by changing source and drain terminals. (a) PFETs with neutral-SL over e-SiGe, (b) PFETs with compressive-SL over e-SiGe.

TABLE I PIEZORESISTANCE COEFFICIENTS FOR SI(001) SURFACE [6].

Channel		<110>			<100>		
Stress		<110> (l)	<1-10> (t)	<001> (v)	<100> (l)	<010> (t)	<001> (v)
PR coeff.	n*1	-2.6	-1.2	3.9	-7.7	3.9	3.9
(x10^{-4}/MPa)	p*2	5.35	-5.85	0.1	-0.6	0.1	0.1

*1: 1x10^{17}cm^{-3}, *2: 5x10^{17}cm^{-3}

TABLE II SUMMARY OF MST IN THIS WORK.

	NFET	PFET
MST Performance enhancement (w.r.t. single-stressor)	Tensile-SL / Poly-stressor > +15%	Compressive-SL / e-SiGe > +18%
Issues	- Stress controllability - Gox reliability	- Degraded I_{on} at narrow W
	- Layout-dependent stress variation - Layout-dependent stress non-uniformity	