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Large Reduction in Standby Power Consumption Achieved with Stress-controlled SRAM Cell Layout

H. Kudo, K. Ishikawa, R. Tanabe, H. Fukutome, Y. Mishima, S. Satou, T. Sugii
F. Kihara [a)], M. Okamoto [a)], M. Yoshimura [a)], T. Sugimachi [a)], H. Hashimoto [a)], M. Ohtsuki [a)]
FUJITSU LABOTARORIES LIMITED, [a)] FUJITSU LIMITED
50 Fuchigami, Akiruno, Tokyo, 197-0833, Japan. E-mail: kudo.hiroshi@jp.fujitsu.com

Abstract

We increased compressive strain in specific active regions by introducing a shallow trench isolation (STI) spacer for a divided SRAM cell layout. The result was a reduction in the IS and an improvement in its variance. We achieved these improvements by controlling the boron diffusion rate and electron mobility. We were thus able to achieve an 80% reduction in standby leakage without increasing the cell size. The simulation indicated that the effect of the STI spacer will also be applicable to the next-generation low standby power (LSTP) transistors.

Introduction

The SRAM in a system LSI occupies most of the chip area and consumes most of the standby power. The straight-type SRAM, which has a straight active region, has a large alignment margin in photolithography, so it is more suitable for integration. However, this type has a large IS as well as its variance, so it cannot satisfy the ITRS requirements for LSTP applications (ITRS 2005 edition). In a novel solution to this problem, we turned our attention to the stress generated by STI. We have reduced IS and its variance by using STI stress to effectively strain the Si in the channel.

SRAM cell layout for IS reduction

Divided and straight types of SRAM cells are illustrated in Fig. 1. The divided type we propose features an active region that is divided by an STI spacer inserted between adjacent unit cells. The insertion of the STI spacer effectively strains the Si lattice of the channel region, thus reducing the IS and its variance. The active regions divided by the STI spacer are connected by a shared contact. The divided type and the straight type have the same cell size. The driver and transfer transistors have respective gate lengths of 0.18 um and 0.27 um. These long gates make it easier for us to clarify whether the IS reduction is due to the STI stress or side-effects such as a gate length shift.

Control of boron diffusion

The standby leakage of the divided cell layout was 80% lower than that for the straight type (Fig. 2). The leakage components of driver and transfer transistors are shown in Fig. 3. The decrease in the effective Ioff of the divided type was due to the reduction of the IS. The IB, which is caused by gate-induced drain leakage (GIDL), was slight. The variance in IS for driver transistors over the wafer is shown in Fig. 4(a). The variance in the IS of the straight type was large, while that for the divided type was small. As shown in Fig. 4(b), the standard deviation of IS for the straight type is 4 times as high as for the divided type.

The depth distribution of implanted boron (B) in the channel is shown in Fig. 5. We ran simulations based on the implantation and annealing conditions used in this work. The annealing process lowered the B concentration peak, and the concentration on the substrate surface decreased from 1.3E18 to 8E17/cm^3. Impurity profile observation using STM is useful for analyzing electric characteristics of transistors [1]. The results of using STM to analyze the B distribution on the active region are shown in Fig. 6. The gate electrode is in the region surrounded by the dotted line in the figure. The STM observation was done after gate oxidation and removal of the gate oxide. The concentration range was found to be from 5E17 to 2E18/cm^3, which is in rough agreement with the simulation results. For the divided type, the gate electrode was placed in the active region about 0.16 um away from the STI spacer. The B concentration in this region was high, while for the straight type, most of the region was low in B concentration. This difference in concentration was caused by the diffusion rate of B; the B diffusion rate is low in the region in which the B concentration is high and high in the region where the B concentration is low. The high IS of the straight type seen in Fig. 3 was due to the low B concentration in the active region. In addition, the large variance of the IS of the straight type seen in Fig. 4 was due to the high B diffusion rate. When the diffusion rate is high, the statistical variance of the dopant in the depth direction is large. This difference in diffusion rate originates in compressive stress that is applied to the active region by the STI spacer in the thermal process. The biaxial compressive strain in Si reduces the B diffusion rate [2]. The 3-D simulation results for distribution of Si strain due to stress in the x- and y-axis directions during gate oxidation process above 900 C are shown in Fig. 7. Insertion of the STI spacer applies a compressive stress in the spacer's vicinity from the x- and the y-axis directions, generating the biaxial compressive strain.

Control of electron mobility

For driver transistors, the change in IS with respect to Vth is shown in Fig. 8. Comparing the IS of the two types of cell layouts at the same Vth revealed that the IS of the divided type was 70% lower than that of the straight type. The difference in the IS trend with respect to Vth seems to have been caused by a change in electron mobility. The drive current of the straight type was 14 % higher than that of the divided type. The change in mobility stemmed from the Si strain caused by the compressive stress from the STI spacer. The same IS as for the divided type can be obtained for the straight type if the dose amount of the channel impurity is increased. However, such a dose increase would degrade the characteristics of the transistors in the circuits of modules other than the SRAM.

We analyzed the Si strain in the gate length direction in the vicinity of the driver transistor using TEM-NBD analysis (Fig. 9). Strain in the gate length direction has a large effect on electron mobility [3]. For the divided type, insertion of the STI spacer created large compressive strain up to the region directly below the gate electrode. The strain stood at -0.5%, which is comparable to that of SiGe epitaxial growth [2]. For the straight type, no large strain was generated. This difference in strain affects the electron mobility and thus causes reduction in IS.

The results of simulations of strain in the gate length direction for 45-nm node SRAM are presented in Fig. 10. For the divided type, the compressive stress from the STI spacer was effective and a high compressive strain was observed. As shown in Fig. 11, the STI spacer will also be effective for the next-generation LSTP transistors. The channel center strain in the divided type was 3.6 times higher than that in the straight type.

Conclusion

We increased compressive strain in specific active regions by introducing an STI spacer for a divided SRAM cell layout. The result was a reduction in the IS and an improvement in its variance. We achieved these improvements by controlling the boron diffusion rate and electron mobility. We were thus able to achieve an 80% reduction in standby leakage without increasing the cell size. This method does not require any change in the ion implantation or other process conditions, so it has no negative effects on the transistor characteristics in circuit modules other than SRAM. The simulation indicated that the effect of the STI spacer will also be applicable to the next-generation LSTP transistors.

References

[1]H. Fukutome, et al., Symp. VLSI Tech., pp.140 (2005).
[2]A. Antonelli et al., Mater. Res. Soc. Symp. Proc. 163, 523
(1990).
[3]K. Goto, et al., IEDM Tech. Digest, 209 (2004).

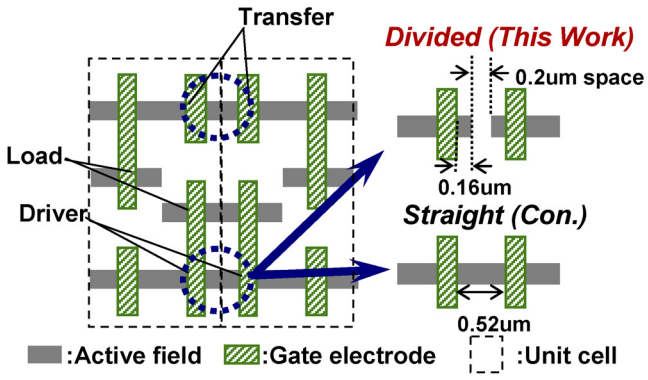


Fig. 1. Structure of the SRAM cell layouts examined in this work.

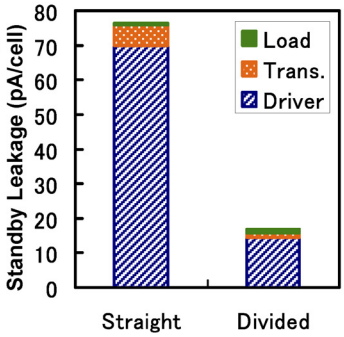


Fig. 2. Standby leakage current for straight and divided cell layouts.

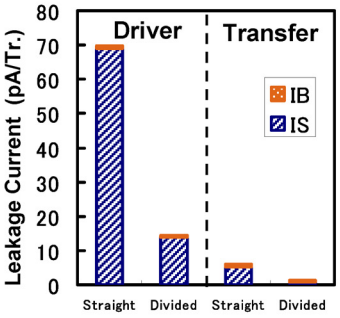


Fig. 3. Leakage components of driver and transfer transistors.

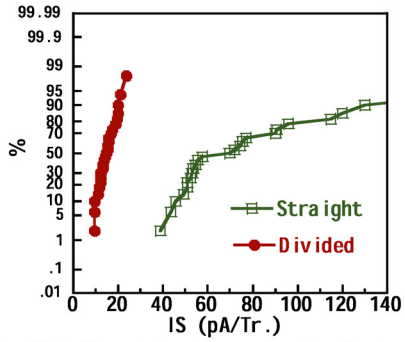


Fig. 4(a). Cumulative frequency distributions of IS for driver.

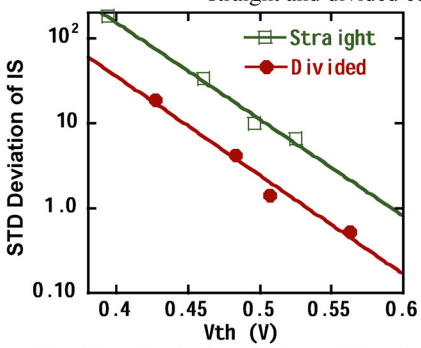


Fig. 4(b). Standard deviation of IS with respect to Vth.

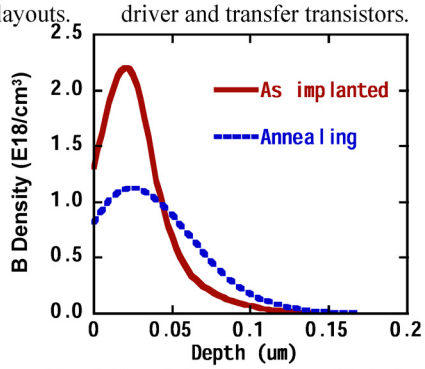


Fig. 5. Simulated B depth profile before and after Annealing.

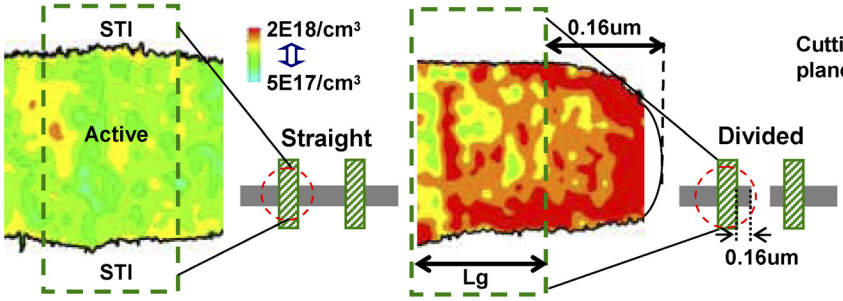


Fig. 6. STM images of p-type impurity (boron) on active field of driver transistors.

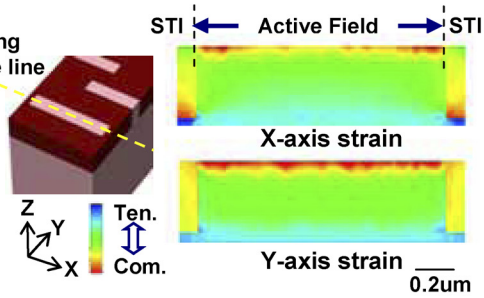


Fig. 7. 3-D simulated distribution of Si strain in direction of x- and y-axes around STI spacer during gate oxidation above 900°C.

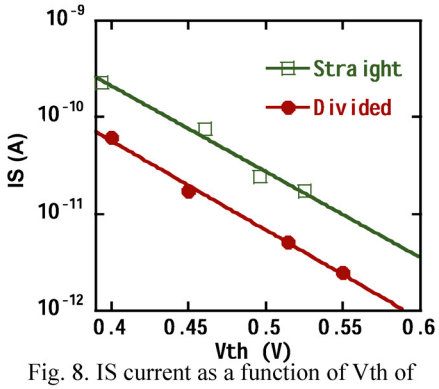
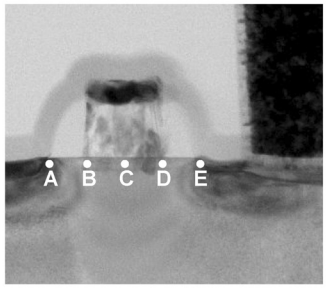


Fig. 8. IS current as a function of Vth of driver transistor.



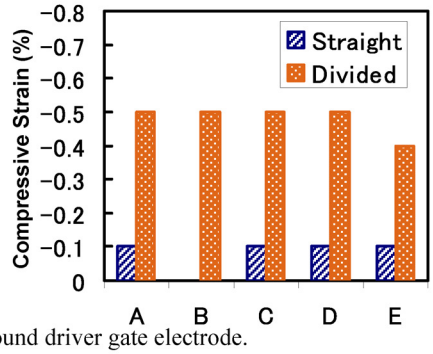


Fig. 9. Comparison of Si strain around driver gate electrode. Marks labeled with Roman letters in TEM image are strain measurement points.

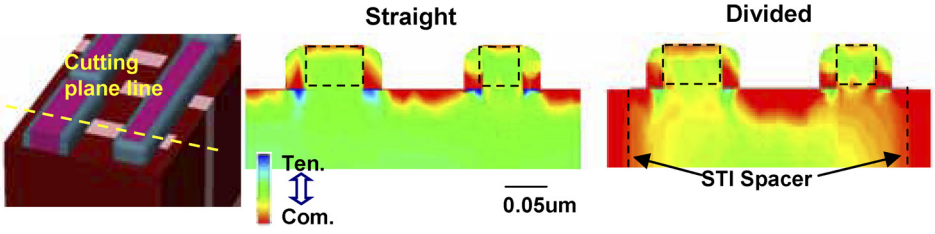


Fig. 10. 3-D-simulated Si strain distribution in direction of gate length for 45-nm node straight- and divided-type SRAM.

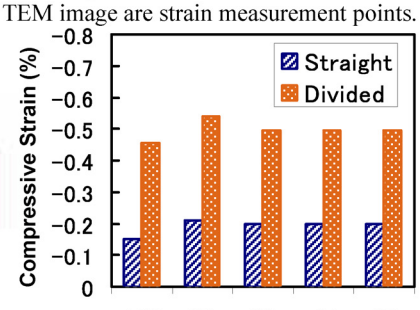


Fig. 11. Si strain change in direction of gate length at channel center with technology node up to 32 nm.