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Layout Independent Transistor with Stress-controlled and Highly Manufacturable STI Process

K. Horita, M. Ishibashi, H. Umeda, T. Kawahara, T. Ikeda, T. Yamashita, T. Kuroi and Y. Inoue

Process Technology Development Div., Renesas Technology Corp.

4-1 Mizuhara, Itami, Hyogo 664-0005, Japan

Phone.:+81-72-784-7322 Fax:+81-72-780-2693 E-mail: horita.katsuyuki@renesas.com

1. Abstract

A fully stress-controlled STI process has been proposed for 45nm technologies and beyond. This process uses single layered SOD (Spin-On Dielectric) film for the gap-filling without employing complicated hybrid structure. With this technique, the mechanical stress caused by STI has been dramatically suppressed. Moreover, drain current (Id) modulation due to STI stress is minimized.

2. Introduction

The strain engineering has become an indispensable technique to improve CMOS performance [1]. Especially, local or uni-axial stress has been recognized to be very effective in the viewpoint of both process simplicity and performance at actual high electric field [2,3]. On the other hand, there exist many kinds of unintentional stress effects on a chip represented by STI related bi-axial stress [4,5]. In actual LSI pattern, there exist many types of transistor layout in spite of same Lg/Wg as shown in Fig.1. The transistor performance depends on the layout pattern due to the bi-axial stress from STI. In order to avoid interferences with the precious local strain, the undesired stress from STI should be suppressed.

Recently, in order to fill the STI narrow gap under 100nm with dielectrics, polysilazane-based SOD process has been introduced instead of conventional HDP process, thanks to its gap-filling ability [6]. There, polysilazane film should be transformed into SiO_2 and hardened through the whole film homogeneously by annealing during STI formation process. However, conventional SOD-STI process essentially has a serious problem of inhomogeneous curing dependent on SOD coating profile. Fig.2(a) shows the schematic views of inhomogeneous curing caused by the difference of SOD film thickness which depends on the trench width. Imperfectly cured film has so high wet-etching rate as shown in Fig.3 that STI shapes scatter and it results in step heights variation between STI SiO_2-surface and active area Si-surface. To avoid this difficulty, the HDP/SOD hybrid STI has been proposed [6,7], however, it diminishes process simplicity and strain fluctuation controllability.

This paper introduces a novel process to resolve these problems with keeping process simplicity and putting in strain controllability. Especially, STI-originated mechanical stress is so effectively suppressed and controlled to zero, that we can concentrate on the intentional strain engineering without considering STI factors of patten-dependent mobility moduration and so forth.

3. Experimental Results and discussion

In order to overcome these difficulties mentioned above, the 2-step-cure process has been employed, where neither HDP cap layer nor etch-stop nitride liner is necessary. The process needs only one additional step of curing process after SOD film polishing to conventional SOD-STI flow, as indicated in Fig. 2(b).

Fig. 4 shows SEM photographs of SOD filled 100nm or 70nm opening STI structure after gate electrode formation compared with wide space, using the conventional processes without second curing step after CMP. In spite of proper step-height in wide width trench, large grooves are generated in narrow trench due to the high wet-etching rate. This issue can be solved adopting the HDP/SOD hybrid process, but it results in the fluctuation of transistor characteristics by changing of STI induced stress [7]. Fig. 5 depicts STI structure after gate electrode formation with novel 2-step curing process. The dependence of STI step-height on the trench width has been remarkably reduced in comparison with that of conventional SOD process.

To evaluate the layout dependence of transistor performance caused by STI stress, simple and stress sensitive transistor patterns, which have differently sized diffusion area, have been measured. Fig. 6 indicates Normalized Id, Vth and transconductance *gm* at several LOD(length of diffusion area). LOD is defined as a diffusion area length between source and drain. In the case of HDP process, Id of NMOS decreases with reducing the LOD. This is due to the degradation of electron mobility by compressive stress of HDP film and volume expansion of STI during oxidation step. On the contrary, Id increases with reducing the LOD in the case of hybrid process. In addition to the tensile stress from SOD film, the nitride liner suppresses the compressive stress generation during oxidation step. As a result, strong layout dependence in the opposite direction still exists. In the case of our 2-step curing process, almost no dependence of Id on LOD has been observed. The STI induced stress is minimized successfully because the oxidation induced compressive stress and the SOD originated tensile stress become almost equivalent in total under the optimized curing condition.

In PMOS transistors, the mobility shift that comes out in gm caused by stress is smaller and has opposite direction in comparison with NMOS. In addition to the mobility modulation, it has been reported that compressive stress suppresses dopant diffusion of Source/Drain extension and halo implantation and in contrast tensile stress accelerates diffusion of impurities [8]. Therefore, Vth shift occurred as described in Fig.6. This Vth shift enhances Id changing in NMOS but it neutralizes in PMOS.

To evaluate stress generation in channel region directly, the Raman spectroscopy analysis is carried out. The evaluated stresses of the conventional HDP sample, the hybrid one and the 2-step-curing SOD one are indicated in Fig. 7. Contrary to compressive stress of the conventional HDP sample, the hybrid one has tensile stress at every measuring point. This is consistent with the results of the dependence of transistor characteristics on LOD described above. It should be noted that the stress from 2-step-curing STI is successfully controlled into the middle state between the HDP sample and the hybrid sample by optimizing curing condition in terms of stress distribution.

These results ensure that modulation of transistor performance by stress is effectively eliminated, so the dependence of transistor characteristics on the pattern layout in LSI is sufficiently suppressed.

The defect inspection of SRAM cell array including very narrow trench has been performed as shown in Fig. 8. The Id modulation hardly depends on curing temperature between 700C and 800C. However, in the case of 700C, the defect density is high because SOD film is imperfectly cured. Curing with 750C or higher, it becomes comparable to conventional HDP process without generating major compressive stress.

This novel technology is evaluated as a 45nm-node CMOS platform. The Vth of SRAM transistor also maintains small slope below 60nm as given in Fig. 9. Both intra- and inter- well isolation property are sufficient for 45nm node isolation as shown in Fig. 10 and 11. This technology is the most promising candidate for 45nm node isolation scheme.

4. Conclusions

A novel technique to manufacture LSIs with layout independent transistors has been proposed. Employing quite simple STI process using SOD film with optimized 2-step-curing method, STI originated mechanical stress has been effectively suppressed. As a result, the layout-dependence of characteristics has been eliminated well.

References

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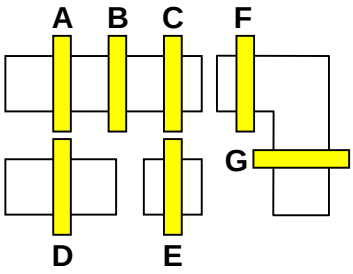

Figure 1 Probable transistor layouts. All transistors (A to G) have same Lg and Wg, but different performance under the STI induced bi-axial stress.

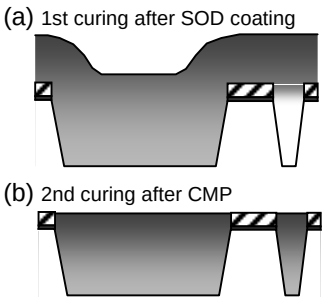

Figure 2 Schematic illustrations of cured areas of SOD film after each steps of 2-step-curing. Dark region indicates SOD film converted from polysilazane into SiO_2.

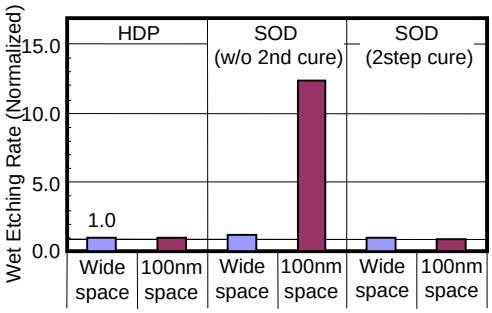

Figure 3 Wet etching rate of SOD films on wide or narrow trench pattern. Wet etching rates are normalized by the rate of HDP film on wide space.

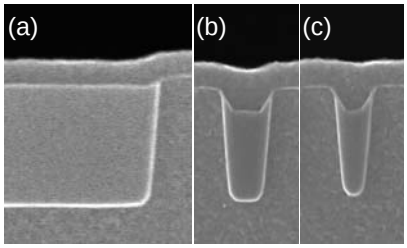

Figure 4 Shapes of conventional SOD filled STI without 2nd cure step. (a)wide space, (b)100nm space and (c)70nm space after dual gate oxide formation.

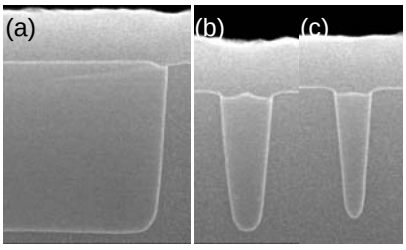

Figure 5 Shapes of SOD filled STI with optimized 2-step-curing method. (a)wide space, (b)100nm space and (c)70nm space after dual gate oxide formation.

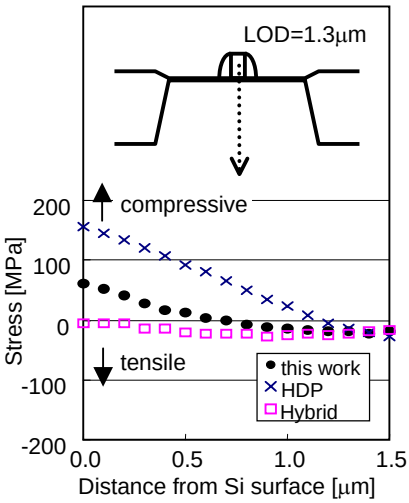

Figure 7 Direct stress measurement of channel region with Raman spectroscopy. Beam is scanning down from surface to bulk along longitudinal axis.

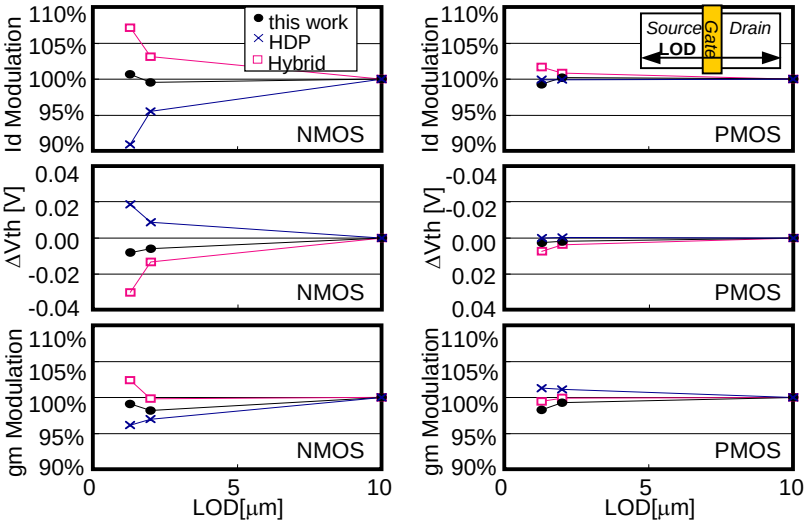

Figure 6 Dependence of Id, Vth, gm on LOD(Length of Diffusion Area) for the transistors fabricated with three types of STI process. NMOS Id is very sensitive for mechanical stress from STI.

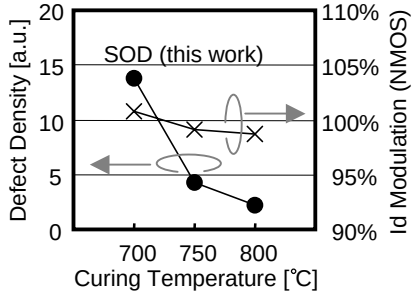

Figure 8 Defect density normalized by HDP case and NMOS Id modulation related to the 1st curing temperature. The curing condition can be optimized in terms of defect density.

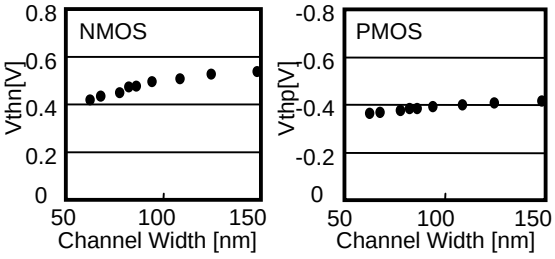

Figure 9 Inverse narrow channel effect of ultra narrow transistors for 45nm node SRAM devices.

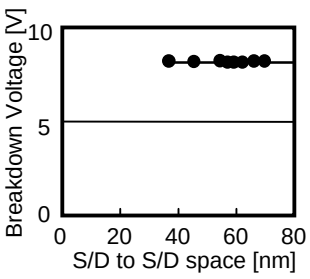

Figure 10 Intra-well isolation characteristics.

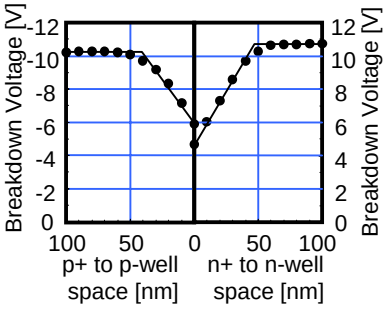

Figure 11 Inter-well isolation characteristics