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A Full Analytical Model to evaluate Strain Induced by CESL on MOSFET Performances

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Abstract

In this paper we propose an analytical approach to model the CESL induced strain MOSFETs, as well as electrical dependence with the gate length.

1. Introduction

Today CESL induced strain is usually used in MOSFET fabrication to enhancement electrical performances. It consists on depositing an intrinsically stressed SiN liner over the MOSFET to induce a stress in the channel device. Literature [1, 2] has been reported about +15% current variation for short gate length devices. This current variation can be related to the carrier mobility dependence on stress, that is commonly known as piezoresistivity effect. Nevertheless the current gain depends on the device layout: gate length, gate height, gate-to-isolation distance… So we propose in this paper an analytical model to evaluate the CESL induced strain impact on the MOSFET electrical performances taking into account the gate length dependence. This approach is based on mechanical considerations, and uses the simple piezoresistivity model. We extract the mobility variation in the strained channel device as a function of the gate length. We introduce this gate length dependence no-uniform mobility in the MASTAR model (Model for ASsessment of CMOS Technologies And Roadmaps) [3], and finally we evaluate the stress impact on the saturation current *Ion* (figure 1).

2. Mechanical simulations – Analytical expression of the stress

Using a 2D-Mechanical Finite Element (MFE) solver, we study how the stress propagates from the intrinsic strained CESL into the MOSFET channel. In these simulations we assume a plane strain, therefore the σ_{yy} component of the stress tensor (along the MOSFET width) is considered to be null. This assumption can be justified by the fact that we take into account a very large transistor, neglecting the active area width dependence of the stress. Moreover simulations have shown that the shear stress components are negligible in the transistor channel. Finally the stress tensor can be reduced to only 2 components σ_{xx} (along the channel length) and σ_{zz} (along the gate height). Figure 2-left shows the σ_{xx} stress component induced by a tensile 1GPa 20nm CESL in a very long device. We can observe that quasi all the structure is in compression; this stress is due to the relaxation of the nitride liner initially tensile. But a small area around the channel edge is tensile. This small area called "stress pocket" is due to the CESL topology in the corner between the spacers and the source/drain areas. Moreover figure 2-right shows the σ_{zz} stress component induced by the same CESL: the stress pockets are high compressive, whereas the stress in the channel tends to disappear. From these MFE simulations, we extract the different stress components σ_{xx} and σ_{zz} along the A-A' axis (defined in figure 2) for several gate lengths L_g (figure 5). The position under the gate is noted x. Stress is not uniform in the channel –stress pocket around the channel edges – and stress depends on L_g: stress increases when L_g decreases. From the long device (2µm gate length) numerical data, we extract the stress variation in one channel edge (figure 4): the effect of only one stress pocket is isolated. The appropriate analytical function to fit these data is given by the eq. (1):

$$\sigma_i(x) = \frac{\sigma_0^i}{1+\left(\frac{x}{L_s^i}\right)^{k_i}} + \sigma_\infty^i \qquad (1)$$

where σ_∞^i is the stress component in the channel, $\sigma_\infty^i + \sigma_0^i$ is the stress in the stress pocket, L_s^i is the stress pocket length and k_i refers to the stress gradient; the *i* sub- or superscript refers to the *xx* or *zz* subscript of the stress component σ. Figure 4 confirms that the eq. (1) is always valid whatever the considered stress component.

It becomes easy to add the effect of the second symmetric stress pocket using superposition theorem. But using this method, the stress induced by the CESL on the top of the gate is counted 2 times. Therefore in order to correct the stress value, we introduce $\sigma_{correction}^i(L_g)$ which is also L_g dependent. MFE simulations show that $\sigma_{correction}^i(L_g)$ follows also an expression equivalent to (1). Finally the stress components depend on both L_g and x, and can be approximated by the eq. (2):

$$\sigma_i(x,L_g) = \sigma_0^i\left(\frac{1}{1+\left(\frac{x+\frac{L_g}{2}}{L_s^i}\right)^{k_i}} + \frac{1}{1+\left(\frac{-x+\frac{L_g}{2}}{L_s^i}\right)^{k_i}}\right) + \sigma_\infty^i\left(1+\frac{1}{1+\left(\frac{L_g}{2L_s^i}\right)^{k_i}}\right) \qquad (2)$$

Figure 5 shows that we have a very good agreement between MFE data and stress evaluated by the eq. (2).

3. Mobility Variation

The stress variation expression (2), coupled to the simple piezoresistivity model eq. (3), permits to determine the variation of the carrier mobility enhancement $K_\mu(x,L_g)$. This mobility law is given by the eq. (3):

$$K_\mu(x,L_g) = \frac{\mu_{strain}(x,L_g)}{\mu_{relax}} = (1-\Pi)\cdot\sigma(x,L_g) \qquad (3)$$

where $\mu_{strain}(x,L_g)$ and μ_{relax} are respectively the carrier mobility in strained and relaxed Si, and Π is the piezoresistivity tensor. In order to simplify expressions, we assume that the different parameters σ_∞^i, σ_0^i, L_s^i and k_i are equivalent for all stress components σ_{xx} and σ_{zz}. Therefore the carrier mobility enhancement can be written as the eq. (4):

$$K_\mu(x,L_g) = \left(K_\mu^{pocket}-1\right)\left(\frac{1}{1+\left(\frac{x+\frac{L_g}{2}}{L_s}\right)^{k}} + \frac{1}{1+\left(\frac{-x+\frac{L_g}{2}}{L_s}\right)^{k}}\right) + \left(K_\mu^{channel}-1\right)\left(1+\frac{1}{1+\left(\frac{L_g}{2L_s}\right)^{k}}\right)+1 \qquad (4)$$

where $K_\mu^{pocket} = \frac{\mu_{pocket}}{\mu_{relax}}$ and $K_\mu^{channel} = \frac{\mu_{channel}}{\mu_{relax}}$ with μ_{pocket} and $\mu_{channel}$ respectively the mobility in the stress pocket and in the channel for a long device. It appears clearly that due to high stresses in the stress pockets compared to the channel residual stress, the mobility enhancement is more important in the stress pockets. Consequently the stress pockets are at the origin of current variation: longer the device is, smaller the stress pocket impact is, and the current variation will be reduced. At the contrarily, smaller the device is and more the current is impacted by the stress pocket. To quantify the stress impact on current, we have to consider a MOSFET with a x position and gate length L_g dependant mobility $\mu(x,L_g)$. In this case, the mobility term in the standard current expression is simply multiplied by a factor $\beta_\mu(L_g)$ eq. (5):

$$I = C_{ox}\beta_\mu(L_g)\mu_{relax}\frac{W}{L_g}\left(V_{gt}-\frac{V_{ds}}{2}\right)V_{ds} \quad ; \quad \beta_\mu(L_g) = \frac{L_g}{\mu_{relax}\int_0^{L_g}\frac{1}{\mu(x)}dx} \qquad (5)$$

The expression (5) indicates that the channel current is limited by the worst mobility area. From expression (5) coupled to the mobility law eq. (4), we can extract the "mean" mobility gain as a function of the gate length L_g (figure 6). This mobility variation behavior has the same characteristics than the experimental data given by [4]. As we can expect, the "mean" mobility variation

increases when the gate length decreases: low mobility stress in the channel les and less impacts the carrier transport. Finally when the stress pockets are totally overlapped, for $L_g < L_s$, the stress is maximum and saturates, and finally $\beta_\mu(L_g)$ saturates. Finally it is possible to reproduce exactly with only 4 fitting parameters the CESL induced stress mobility dependence in the channel MOSFET.

4. Current Performance Variation

The factor is introduced in the MASTAR model [3], and coupled to the expression (4), to evaluate the stress impact on the MOSFET saturation current *Ion*. In first time our model is validated by experimental data: figure 8 shows nMOSFET *Ion* variation for different CESL compared to a nMOSFET with a stress-less CESL. It appears clearly that whatever the used CESL (compressive or tensile, thickness, intrinsic strain…), there is a very good agreement between our model and the experimental data. The used parameters to fit the experimental data are given in figure 7. The stress pocket extension is evaluated to 80nm for tensile CESL and 180nm for compressive CESL. Moreover thicker the CESL is, and greater the stress in the stress pocket is, which is traduced by a greate for tensile CESL (better mobility), and a lower for compressive CESL (worst mobility).

The saturation current variation (figure 8) is maximal around 100nm gate length. This length is characteristic to the stress pocket extension L_s : the stress induced in the channel is maximal due to the complete overlap of the 2 stress pockets, and a maximal "mean" mobility variation. Longer devices have a smaller *Ion* variation due to a lower: the lower stress in the middle of the channel does not induce an important mobility variation, and finally the current is limited by transport in this area. Sub-100nm gate length devices show also a reduction of the current variation. This behavior can be related to the current dependence on saturation velocity: indeed the gate length reduction implies that the saturation current is less and less limited by carrier mobility and more and more limited by saturation velocity. Finally the mobility variation is partially transmitted to saturation current. For smaller devices, the ~80% of carrier mobility is converted to only 10% of drive current enhancement. As illustration, figure 9 shows the different current enhancement asymptotes to highlight this typical behavior.

5. Conclusion

We have developed a model to understand the origin of the drive current enhancement when we applied a stress in the CESL. This model can predict with very good agreement with experimental data, the impact of the CESL induced stress on the MOSFET electrical performances. This model is based on a physical approach which allows optimizing CESL process fabrication to obtain the optimal stress efficiency.

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References:

[1] F. Boeuf, et al., SSDM'05
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[3] T. Skotnicki, et al., ECS Conference'02, Full MASTAR Model
Available at http://itrs.public.net. See ITRS 2003 Edition, p.311
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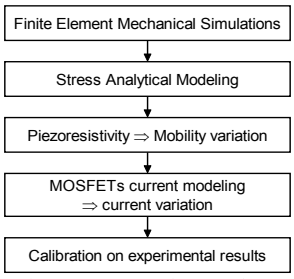

Figure 1: Approach to evaluate stress impact on MOSFET

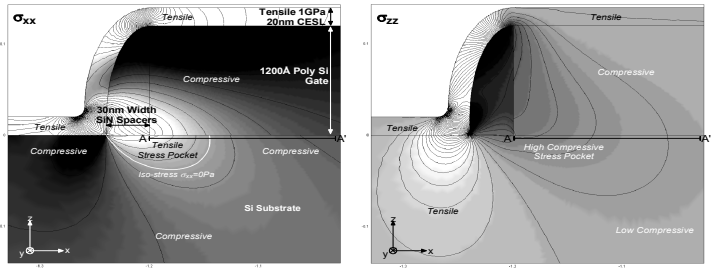

Figure 2: σ_{xx} (left) and σ_{zz} (right) components induced by a tensile CESL on a long MOSFET. A "stress pocket", is localized around the channel edge.

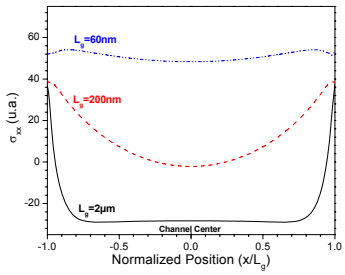

Figure 3: Stress component σ_{xx} calculated by MFE simulations

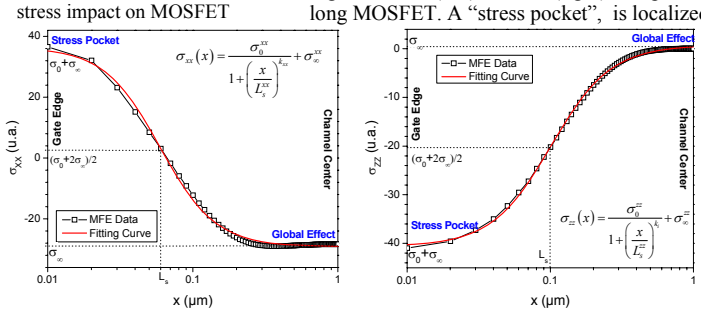

Figure 4: σ_{xx} (left) and σ_{zz} (right) stress - symbols: MFE data extracted along the A-A' axis, lines: the fitting curves are given by eq. (1).

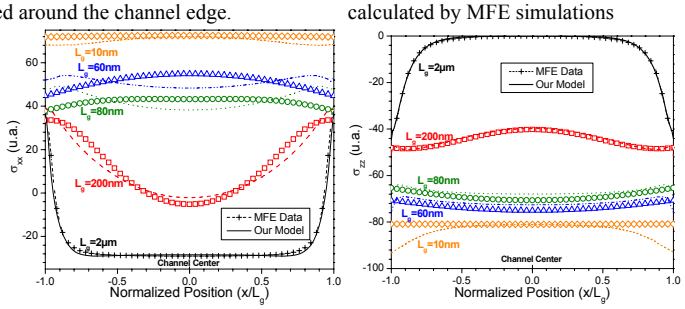

Figure 5: σ_{xx} (left) and σ_{zz} (right) profile in the channel MOSFET for different gate lengths L_g. The fitting curves are given by eq. (2).

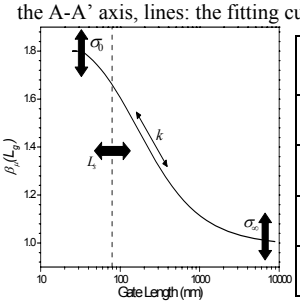

Figure 6: "Mean" mobility variation $\beta_\mu(L_g)$ and the effect of the different parameters σ_∞ , σ_0 , L_s and k .

	K_μ^{pocket}	$K_\mu^{channel}$	L_s (nm)	k
800Å Tensile +960MPa CESL	1.45	0.99	80	1.7
1500Å Tensile +960MPa CESL	1.58	0.99	80	2.2
800Å Compressive +960MPa CESL	0.71	1.04	180	2.7
1500Å Compressive +960MPa CESL	0.66	1.04	180	3

Figure 7: Fitting parameters used to reproduce experimental data for several CESL (compressive or tensile CESL and different thicknesses).

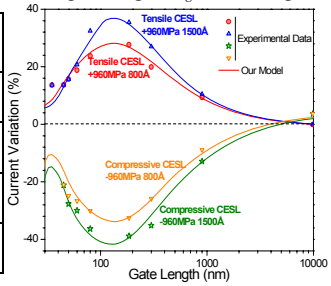

Figure 8: nMOSFET *Ion* variation as a function of L_g for several CESL (compressive or tensile CESL and different thicknesses).

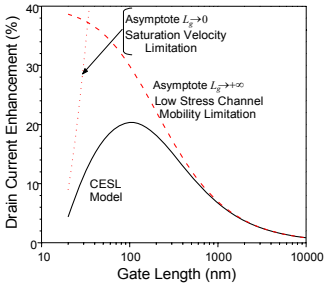

Figure 9: Limitation of the current enhancement by mobility in the low stress channel for long devices, and by saturation velocity for sub-100nm devices.