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56% pMOSFETs Drive Current Enhancement from Optimized Compressive Contact Etching Stop Layer (CESL) for 45nm Node CMOS

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Abstract

With further optimizing the conventional compressive CESL, the record 56% drive current gain of pMOSFETs has been first demonstrated instead of high cost and complex SiGe process. Compared to conventional compressive CESL performance, this optimized film also provides an extra 24% current gain on pMOSFETs, which far derivates from the trend of the drive current gain on the integrated film stress.

Introduction

As downscaling the CMOS device dimension reaches its fundamental limits, the enhancement of carrier mobility has been widely researched by introducing strain technology into the channel region. The local strain techniques by using tensile and compressive nitride CESL (Contact-Etch-Stop-Layer) films were introduced to improve electron mobility for nMOSFETs and hole mobility for pMOSFETs, respectively [1-4]. To achieve a higher drive current of pMOSFETs, most studies were also focused on S/D SiGe refill technologies [5,6], but the SiGe scheme suffers from more challenges including complex integration, process control and high cost.

In this study, we addressed on the development of much higher compressive CESL for easier integrated capability. By the breakthrough on the C_CESL (Compressive CESL) modification, higher strain could be more effectively transferred into the channel of pMOSFETs and the record 56% drive current gain can be also reached, competed to the performance of the SiGe scheme. Various electrical, capacitance and reliability characteristics were measured to prove this optimized C_CESL applicability.

Device Preparation

Process flow for the CMOS device is shown in **Fig.1.** The high performance device was fabricated on a <110> P-type substrate. Shallow trench isolation was applied to define device active area and prevent leakage current. Then well and Vt implantations were followed to define the channel profile. After a triple-oxynitride gate process, the poly line was patterned and the transistors were optimized with shallow extensions and S/D RTA. After NiSi process, a compressive nitride CESL film was introduced to enhance the channel strain of pMOSFETs. Control wafers were deposited by conventional nitride CESL film with very low stress. **Fig. 2** shows a cross-section TEM picture of the pMOSFETs device.

Results and Discussion

The normalized drive current (Ion) vs. off current (Ioff) characteristics of the short-channel pMOSFETs has been further enhanced by the presence of an optimized C_CESL layer, as shown in **Fig. 3**. 56% drive current gain is already observed by optimizing the C_CESL, while only 32% drive current gain can be achieved by the conventional C_CESL. The optimized C_CESL film transfers a higher stress into the channel of pMOSFETs and demonstrates an excellent drive current gain. Compared to recent SiGe improvement activities [4-6] listed in **Table 1,** this work shows a competitive drive current gain of pMOSFETs. Besides, this maximum current gain can be achieved only by optimizing C_CESL film deposition without developing new material. Instead of complex integration and huge extra cost by SiGe technology, the optimized C_CESL film becomes the better candidate for pMOSFETs' drive current enhancement.

Fig. 4 shows the dependence of the drive current gain on the integrated film stress for pMOSFETs and higher saturated drive current gain could be obtained by the optimized C_CESL. As the integrated film stress increased over a specific stress, the drive current gain significantly derivates from the liner trend (**Fig. 5**) and the slop speeds up into a superior linear behavior. It is consistent with the previous report [7] that an extreme compressive stress can modulate the bandstructure resulting in more significant hole mobility enhancement with lower hole effective mass and scattering suppression.

Fig. 6 and **7** show the *Id-Vgs* and *Id-Vds* curves of pMOSFETs with Lpoly=38nm, respectively. The swing values of control wafer, conventional C_CESL and optimized C_CESL devices are around 96mV/decade. The comparable Vt roll-off and the DIBL (Drain-Induced-Barrier- Lowering) characteristics are also shown in **Fig. 8** and **Fig. 9**, respectively. In **Fig. 10**, the Gm gain gap of the optimized C_CESL (+140%) is much better than that of the conventional C_CESL (+70%) by a factor of 2. It is believed that the channel hole mobility could be further enhanced successfully by the optimized C_CESL. *C-V* (Capacitance-Voltage) characteristics shown in **Fig. 11** are comparable between different C_CESL film and the control wafers. The results indicated that the process with the optimized C_CESL layer would not induce extra charges trapping in the oxide bulk.

Fig. 12 shows the *Ion-Ioff* characteristics of the test structures with and without dummy poly pattern. Up to 72% drive current gain of pMOSFETs without dummy poly pattern could be obtained by the optimized C_CESL. It is explained that the stress would be suppressed by the dummy poly pattern. **Fig.13** shows a TCAD simulation on dummy poly effect where the dummy poly space is defined from 0.2um to 1.4um. The simulation shows the 9.3% degradation of Sxx (longitudinal way) stress is observed from space=1.4um to 0.3um. That clarifies the current gain offset between the test structures with and without dummy poly pattern. Furthermore, once the space narrower than 0.3um, it will be degraded rapidly to 40% loss as space=0.2um. Thus, the dummy poly pattern also plays an important role in the optimization of the integrated film stress.

Finally, in **Fig. 14,** the NBTI of IO pMOSFETs was also stressed at Vg=-4.4V and 125C. Results show that NBTI degradation for the optimized C_CESL film still keeps the same to the control wafers and traditional C_CESL.

Conclusions

With optimizing C_CESL, the drive current gain of 56% has been successfully demonstrated for 45nm node CMOS, and is extendible to future technologies. In this study, the CESL scheme has proved to be the superior and friendly candidate instead of high cost and complex SiGe process. Compared to conventional compressive CESL performance, this optimized film can also provide an extra 24% current gain on pMOSFETs, which far derivates from the trend of the drive current gain on the integrated film stress.

References

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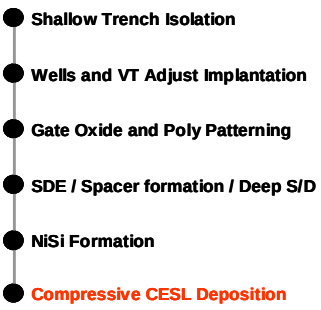

Fig. 1. Standard CMOS process flow.

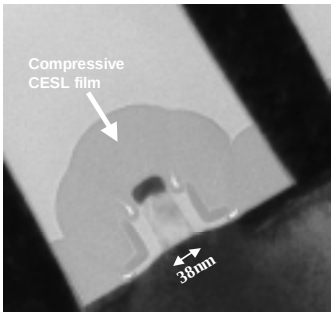

Fig. 2. Cross-section TEM picture of pMOSFETs.

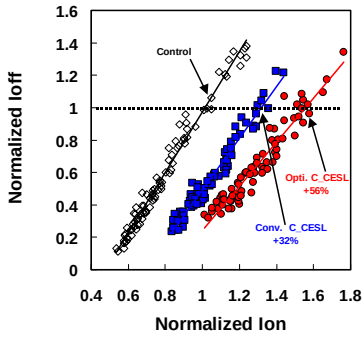

Fig. 3. A 56% drive current enhancement of pMOSFETs with an optimized C_CESL.

	Ref. (4)	Ref. (5)	Ref. (6)	This Work
Vcc	1.0V	1.0V/1.2V	1.0V	1.0V
EOT	---	1.2nm	---	1.2nm
Poly Length	45nm	35nm	40nm	38nm
Scheme	C_CESL	SiGe	SiGe + C_CESL	C_CESL
Ion Gain	+32%	+50%	+53%	+56%

Table 1 Summary of recent C_CESL and SiGe research results.

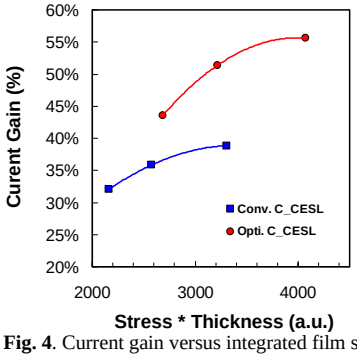

Fig. 4. Current gain versus integrated film stress.

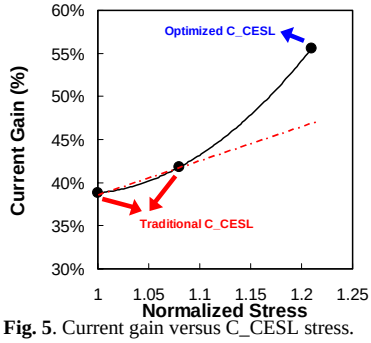

Fig. 5. Current gain versus C_CESL stress.

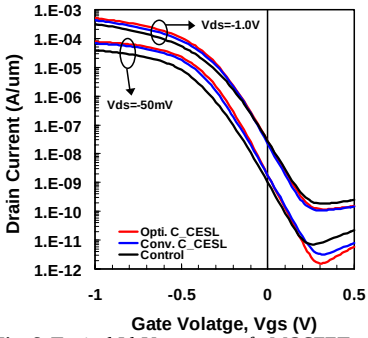

Fig. 6. Typical Id-Vgs curves of pMOSFETs with various C_CESL deposited.

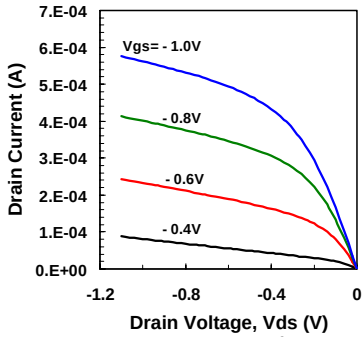

Fig. 7. Typical Id-Vds curves of pMOSFETs with various C_CESL deposited.

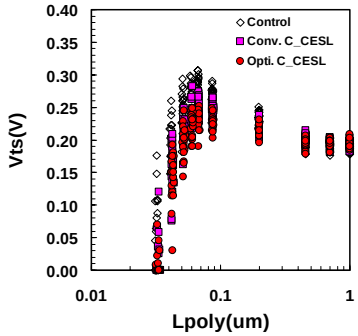

Fig. 8. Measured Vt roll-off for pMOSFETs with various C_CESL deposited.

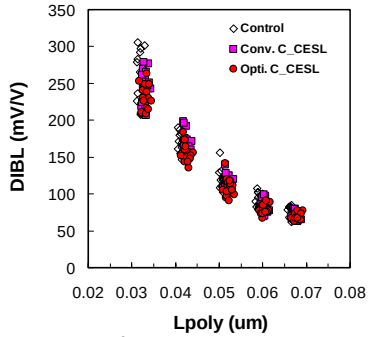

Fig. 9. DIBL of the pMOSFETs depends on different CESL film utilized.

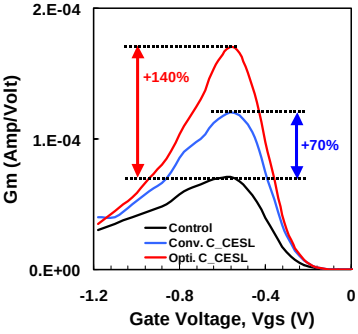

Fig. 10. Gm of the pMOSFETs depends on different CESL film utilized.

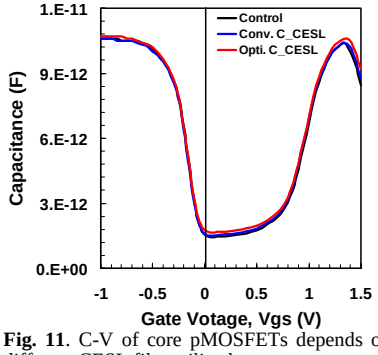

Fig. 11. C-V of core pMOSFETs depends on different CESL film utilized.

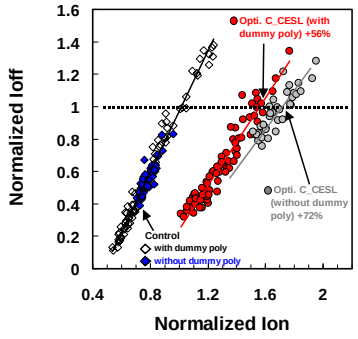

Fig. 12. Ion vs. Ioff characteristics of pMOSFETs with and without dummy poly pattern.

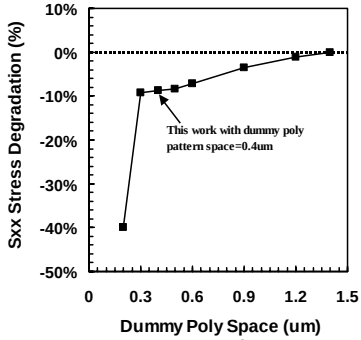

Fig. 13. TCAD simulation of dummy poly space vs. Sxx stress degradation.

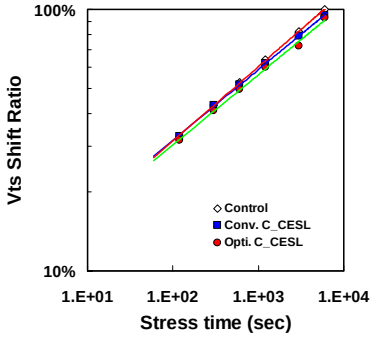

Fig. 14. Vts shift ratio of IO pMOSFETs with stressing at Vg=-4.4V, 125^{0}C for 6000".