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A Continuous, Explicit Drain-Current Model for Asymmetric Undoped Double-Gate MOSFETs

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1. Introduction

Intense efforts are being devoted to the development of compact models for DG-MOSFETs in the literature. The implicit [1–3] and explicit solutions [3–5] for surface potential, ϕ_s of undoped s-DG MOSFETs have been reported, while undoped asymmetric cases have only been solved implicitly in literature [6]. The previous work [6] on a-DG only considers (minor) asymmetry due to workfunction difference (i.e., minimum potential could still be within the channel) as the same gate voltage has been considered on both the gates, and the solutions have to be obtained iteratively. In this paper, we first present a *generic* implicit surface potential solution for undoped a-DG MOSFETs, physically scalable with independent applied gate biases and oxide/channel thickness variations, which can also be extended to SOI MOSFETs. *Explicit* regional solutions are derived for the first time for a-DG and the unified regional solution shows an error in the mili-volts range with respect to the (exact) implicit solutions. Both implicit and explicit solutions converge to the s-DG solution when both gates are identical in all aspects. Finally a continuous, explicit drain-current equation has been derived using the explicit surface potential equation.

2. Analytical Surface Potential and Drain-current Solution

A DG MOSFET structure can be asymmetric due to differences in gate thickness, dielectric material, gate charges, or biases on the two gates. In order to solve the surface potentials explicitly, we start from Poisson's. After some arithmetical transformations, we can get one implicit equation for ϕ_{s1} (not including ϕ_{s2}). For simplicity, the a-DG MOSFET operation can be divided into two regions: subthreshold and strong-inversion regions. In the subthreshold region, the device operates in volume inversion, i.e., the carriers are distributed throughout the entire silicon volume. When both channels are in volume inversion, the electric field in the channel keeps constant. Based on this, the final explicit regional ϕ_{s1} expression in subthreshold is given by

$$\phi_{sub1}=\frac{\dfrac{\varepsilon_{ox1}t_{ox2}}{\varepsilon_{ox2}t_{ox1}}\left(1+\dfrac{\varepsilon_{ox2}t_{Si}}{\varepsilon_{Si}t_{ox2}}\right)V_{gf1}+V_{gf2}}{1+\dfrac{\varepsilon_{ox1}t_{ox2}}{\varepsilon_{ox2}t_{ox1}}\left(1+\dfrac{\varepsilon_{ox2}t_{Si}}{\varepsilon_{Si}t_{ox2}}\right)}. \quad (1)$$

When gate 1 is in strong inversion, surface potential (ϕ_{s1}) is strongly influenced by V_{g1} rather than by V_{g2}. In that case, we get the strong-inversion regional solution as

$$\phi_{str1}=V_{gf1}-2v_{th}\mathcal{L}_{+}\left\{\frac{qt_{ox1}}{\varepsilon_{ox1}}\sqrt{\frac{n_i\varepsilon_{Si}}{2kT}}e^{(V_{gf1}-V_c)/2v_{th}}\right\} \quad (2)$$

where $L_+\{w\}$ is the *Lambert W* function (principal branch). After the potentials are solved analytically in each region, we use the following smoothing function to obtain a unified (explicit) ϕ_s model

$$\mathcal{G}\{\phi_{sub1},\phi_{str1};\delta\}\equiv 0.5\left[\phi_{sub1}+\phi_{str1}+\delta-\sqrt{\left(\phi_{str1}-\phi_{sub1}-\delta\right)^2+4\delta\phi_{str1}}\right] \quad (3)$$

where δ is a smoothing parameter, which is set to a constant 0.001 (which can be tuned for smoothness).

There are four cases of interest for ϕ_{s1} and ϕ_{s2} in different operating (or asymmetry) conditions (either one is biased in volume or strong inversion). When both are in the same mode of operation, it can be solved just by utilizing the above explicit equations. The explicit regional ϕ_{s2} equations are simply arrived at by swapping subscripts '1' and '2' in (1), (2) and (3). When both are in different mode, the behavior of ϕ_{s1} and ϕ_{s2} is a little different. For example, when ϕ_{s1} is in strong inversion and ϕ_{s2} in volume inversion, ϕ_{str2} can be extracted from ϕ_{str1}. We get the ϕ_{s2}

$$\phi_{sub2}=\frac{\dfrac{\varepsilon_{ox2}t_{ox1}}{\varepsilon_{ox1}t_{ox2}}\left(1+\dfrac{\varepsilon_{ox1}t_{Si}}{\varepsilon_{Si}t_{ox1}}\right)V_{gf2}+V_{gf1}}{1+\dfrac{\varepsilon_{ox2}t_{ox1}}{\varepsilon_{ox1}t_{ox2}}\left(1+\dfrac{\varepsilon_{ox1}t_{Si}}{\varepsilon_{Si}t_{ox1}}\right)}$$

$$\phi_{str2}=V_{gf2}-\frac{2v_{th}}{1+\dfrac{\varepsilon_{ox2}t_{Si}}{\varepsilon_{Si}t_{ox2}}}\times\mathcal{L}_{-}\left\{\frac{-qt_{ox2}}{\varepsilon_{ox2}}\sqrt{\frac{n_i\varepsilon_{Si}}{2kT}}\left(1+\frac{\varepsilon_{ox2}t_{Si}}{\varepsilon_{Si}t_{ox2}}\right)e^{(V_{gf2}-V_c)/2v_{th}}\right\} \quad (4)$$

$$\phi_{s2}=\mathcal{G}\{\phi_{sub2},\phi_{str2};\delta\}$$

where $L_-\{w\}$ is the *Lambert W* function (negative branch). If we set the parameters of both gates (bias, oxide thickness, workfunction, etc.) to be equal, then the a-DG equations (1) and (2) will automatically revert to the symmetric case. Finally the drain-current equation is extracted from Pao-Sah's integral, which can be expressed as

$$I_D=\frac{W}{L}\mu\int_0^{Vds}\left(\varepsilon_{ox1}\frac{V_{g1}-\Delta\phi_{i1}-\varphi_{s1}}{t_{ox1}}+\varepsilon_{ox2}\frac{V_{g2}-\Delta\phi_{i2}-\varphi_{s2}}{t_{ox2}}\right)dV \quad (5)$$

By substituting (3) and (4) into (5), we interestingly find that our expressions for ϕ_{s1} and ϕ_{s2} make (5) integrable and therefore a continuous, explicit drain-current equation is reached though it's very long and complicated.

$$I_D=\frac{\mu W}{2L}\left(I_{DA}-\delta V_c\left(\frac{\varepsilon_{ox1}}{t_{ox1}}+\frac{\varepsilon_{ox2}}{t_{ox2}}\right)+I_{DC1}+I_{DC2}\right)\Big|_0^{Vds} \quad (6)$$

$$I_{DA}=-\left(\frac{\varepsilon_{ox1}}{t_{ox1}}\left(\frac{1}{2}(V_{gf1}-\varphi_{str1})^2+\frac{2kT}{q}(V_{gf1}-\varphi_{str1})\right)\right.$$

$$\left.\frac{\varepsilon_{ox2}}{t_{ox2}}\left(1+\frac{\varepsilon_{ox2}t_{si}}{\varepsilon_{si}t_{ox2}}\right)\left(\frac{1}{2}(V_{gf2}-\varphi_{str2})^2+\frac{2kT}{q}(V_{gf2}-\varphi_{str2})\right)\right)$$

$$I_{DC1,2} = -(\frac{2kT}{q} + \frac{1}{2}(\phi_{sub1,2} - \delta - \phi_{str1,2}))\sqrt{(\phi_{sub1,2} - \delta - \phi_{str1,2})^2 + 4\delta\phi_{sub1,2}}$$
$$-[\frac{2kT}{q}(\phi_{sub1,2} - \delta - V_{gf1,2}) + 2\delta\phi_{sub,21}]\times$$
$$\ln(\phi_{sub1,2} - \delta - \phi_{str1,2} + \sqrt{(\phi_{sub1,2} - \delta - \phi_{str1,2})^2 + 4\delta\phi_{sub1,2}})$$
$$+\frac{2kT}{q}\sqrt{(\phi_{sub1,2} - \delta - V_{gf1,2})^2 + 4\delta\phi_{sub1,2}}\times$$
$$\ln\{\frac{4kT}{q}[(\phi_{sub1,2} - \delta - V_{gf1,2})^2 + 4\delta\phi_{sub1,2} + (\phi_{sub1,2} - \delta - V_{gf1,2})(V_{gf1,2} - \phi_{str1,2})$$
$$+\sqrt{(\phi_{sub1,2} - \delta - V_{gf1,2})^2 + 4\delta\phi_{sub1,2}}\sqrt{(\phi_{sub1,2} - \delta - \phi_{str1,2})^2 + 4\delta\phi_{sub1,2}}]/(V_{gf1,2} - \phi_{str1,2})\}$$

3. Results and Discussion

In this section, results of the explicit solutions are compared with the (exact) implicit solutions for various operating conditions. All plots are with $V_c = 0$ unless otherwise stated. Figure 1 shows the unified explicit surface potentials at the two gates, which have less than 4-mV error with respect to the implicit solutions. Subsequent plots further show our ϕ_s model scalability and transitions to SOI/s-DG operations, which indicates that we have captured the essential physics of device operation. Figure 2 demonstrates a-DG operation with channel-thickness variations. Volume inversion and strong inversion for both gates are clearly well predicted by the regional physical expressions, as compared with the exact implicit solutions. Figure 3 plots the model behavior for gate 2 oxide-thickness variations with fixed gate 1 oxide thickness.

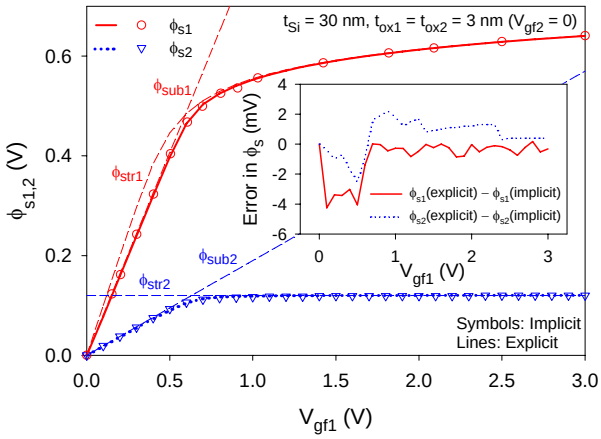

Figure 1. Unified explicit surface-potential solutions and their regional components, compared with the implicit solutions (*symbols*). The inset shows the absolute errors of the explicit solutions.

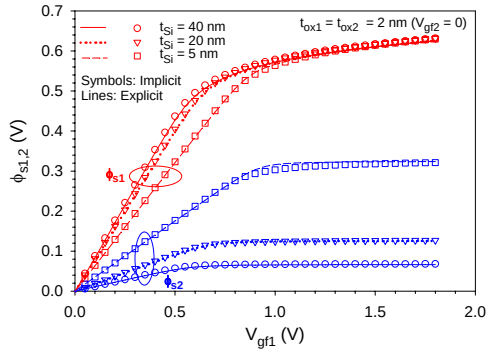

Figure 2. Explicit (*lines*) and implicit (*symbols*) surface-potential solutions with channel thickness variations.

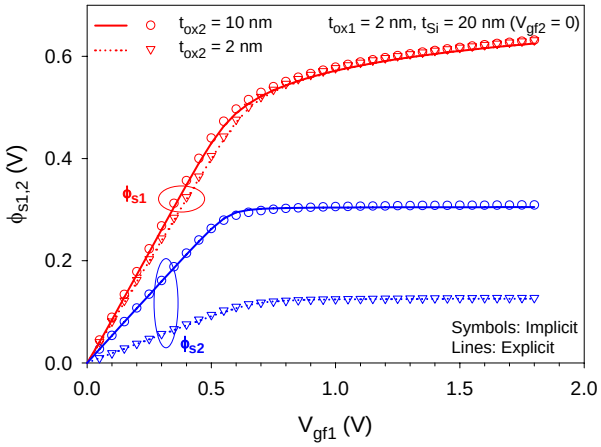

Figure 3. Explicit (*lines*) and implicit (*symbols*) surface-potential solutions with gate 2 oxide thickness variations.

Finally, Figure 4 gives the comparison of the explicit, analytical drain current-drain voltage output characteristics and that from MEDICI results, for four values of gate voltages. The agreement is very good.

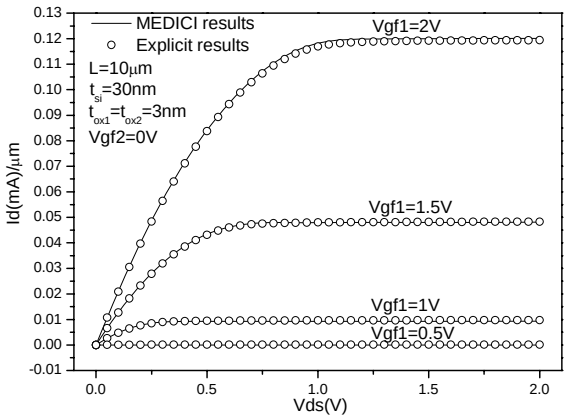

Figure 4. Comparison of the drain current-drain voltage output characteristics as calculated analytically and from MEDICI results, for four values of gate voltages.

Acknowledgements

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