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Surface-Potential-Based MOS-Varactor Model for RF Applications

M. Miyake, N. Sadachika, D. Navarro, Y. Mizukane, T. Ezaki, M. Miura-Mattausch,
H. J. Mattausch[1], T. Ohguro[2], T. Iizuka[2], M. Taguchi[2], S. Kumashiro[2], and S. Miyamoto[2]

Graduate School of Advanced Sciences of Matter, [1]Research Center for Nanodevices and Systems,
Hiroshima University, 1–3–1, Kagamiyama, Higashi-Hiroshima, Hiroshima, 739–8530, Japan
Phone: +81–82–424–7637 Fax: +81–82–424–7638 E-mail: miyake-m053223@hiroshima-u.ac.jp

[2]Semiconductor Technology Academic Research Center, 3–17–2, Shin-Yokohama, Kanagawa, 222–0033, Japan

1. Introduction

Varactors are important for RF circuits as voltage-dependent capacitances, e.g. for frequency tuning of voltage controlled oscillators (VCOs). Among different varactor structures, MOS-based varactors offer a better frequency tuning range and a higher quality factor Q [1].

Different operation modes, either the inversion mode or the accumulation mode, distinguish the MOS varactor type [2]. Inversion-mode MOS varactors are constructed like normal MOSFETs. Accumulation-mode MOS varactors use the same impurity type for source/drain contacts and for the well (see Fig. 1), and thus lack a good source for supplying inversion layer carriers, which have to be generated mainly thermally.

Though importance of the MOS-varactor is very high, accurate models for RF circuit simulation are still missing, especially for the accumulation type. Here we report an accurate surface-potential accumulation-mode MOS varactor model for RF circuit simulations, developed as an extension of HiSIM (Hiroshima-university STARC IGFET Model) [3].

2. Modeling Approach

We evaluate the MOS-varactor model quality with 2D-device simulation, because this method allows to know microscopic device features, which are reliable even for very high frequencies, because 2D-device simulation solves the carrier dynamics explicitly. The investigated MOS-varactor size is fixed to W/L=$1\mu m/2\mu m$, and the impurity profile is fixed to usual literature values, as given in Fig. 1.

The accumulation-mode MOS varactor can be treated as a two-port capacitor. The regions corresponding to source, drain and bulk in conventional MOSFETs are connected together and form the second port besides the gate. At very slow operation, the MOS varactor has the same capacitance characteristic as a normal MOSFET. In RF operation, only the bulk charge is responsible for the capacitance component. Since HiSIM calculates the surface potential, origin of the induced charges, from the accumulation region to the strong inversion region consistently, this bulk charge can be seamlessly calculated without problem.

3. MOS-Varactor Analysis and Modeling Results

Fig. 2 compares the 2D-calculated MOS-varactor capacitance C_{gg} as a function of V_{gb} under the DC condition with the HiSIM-based varactor model. Results of a p-channel MOSFET with the same bulk-impurity concentration are depicted in addition and verify as expected that the capacitance characteristic is also the same.

Fig. 3 shows the C_{gg}-V_{gb} characteristic of the MOS varactor under AC analysis for different frequencies. It should be noted that HiSIM can reproduce 2D device simulation results up to radio frequencies. Beyond 10GHz, calculated capacitances start to decrease with frequency especially in the accumulation region. This reduction is attributed to the bulk-carrier Non-Quasi-Static (NQS) effect [4]. Majority carriers in the bulk contact (and the well) take time to move to the surface at the gate oxide. Therefore, the MOS varactor loses its high capacitance-tuning capability at higher frequencies.

The NQS model of HiSIM considers the majority carrier transit delay τ_{B} (Fig. 4) in the carrier formation as

$$q_{\mathrm{B}}(t_{\mathrm{i}}) = \frac{q_{\mathrm{B}}(t_{\mathrm{i-1}}) + \frac{\Delta t}{\tau_{\mathrm{B}}} Q_{\mathrm{B}}(t_{\mathrm{i}})}{1 + \frac{\Delta t}{\tau_{\mathrm{B}}}};\ \Delta t = t_{\mathrm{i}} - t_{\mathrm{i-1}} \qquad (1)$$

where $q_{\mathrm{B}}(t_{\mathrm{i}})$ and $Q_{\mathrm{B}}(t_{\mathrm{i}})$ represent the NQS and the QS carrier density at time t_{i}, respectively. Fig. 5 shows E_{y}, the depth direction component of the electric field, $10nm$ below the middle of the gate oxide as a function of V_{gb}. The sign of E_{y} controls majority carriers gathering to the surface (accumulate) or departing from the surface (deplete). $|E_{\mathrm{y}}|$ determines the carrier speed for moving, and the carrier transit delay is proportional to the inverse of the speed (see the right axis of Fig. 5). Here two drift delays are distinguished: the accumulation delay τ_{ACC} and the depletion delay τ_{DEP}. τ_{ACC} and τ_{DEP} are modeled by an exponential function with model parameters A to F and the flat-band voltage V_{FB} to take account of the field characteristic shown in Fig. 5. The multiplication with the channel length L includes the L dependence explained in Fig. 4. Finally, τ_{ACC} and τ_{DEP} are combined to obtain τ_{B} by the Matthiessen rule.

$$\tau_{\mathrm{DEP}} = L \cdot \left[A \exp\bigl(B(V_{\mathrm{gb}} - V_{\mathrm{FB}})\bigr) + C\right] \qquad (2)$$

$$\tau_{\mathrm{ACC}} = L \cdot \left[D \exp\bigl(E(V_{\mathrm{FB}} - V_{\mathrm{gb}})\bigr) + F\right] \qquad (3)$$

$$\frac{1}{\tau_{\mathrm{B}}} = \frac{1}{\tau_{\mathrm{DEP}}} + \frac{1}{\tau_{\mathrm{ACC}}} \qquad (4)$$

4. Discussion

The quality factor Q is an important measure for the MOS varactor, and is defined as

$$Q = \frac{1}{2\pi f \cdot R_{\mathrm{p}} \cdot C_{\mathrm{gg}}} \qquad (5)$$

where R_p is the parasitic resistance [1]. Sometimes an inductance L is included in the definition for high frequency analysis. However, we take into account the NQS effect explicitly, so that the simple definition is applicable. Fig. 6 shows Q multiplied by R_p versus frequency at V_{gb}=1V. In a double-log plot, QR_p is proportional to frequency up to 10GHz. At frequencies higher than 10GHz, the Q value starts to deviate from the linear dependence.

5. Conclusion

For RF-circuit analysis, an accurate compact model for MOS varactors is urgently desired. We have developed such an accurate MOS varactor model based on the surface-potential MOSFET model HiSIM. Very good agreement with 2D device simulation result is verified.

References

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[3] HiSIM2.3.0 User's Manual, 2006.

[4] D. Navarro, et al., *SISPAD 2004*, p. 259.

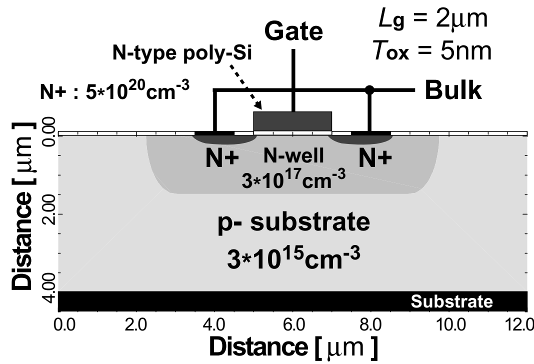

Fig. 1: Cross section of the studied accumulation-mode MOS varactor with n-type well and n-type poly-Si gate.

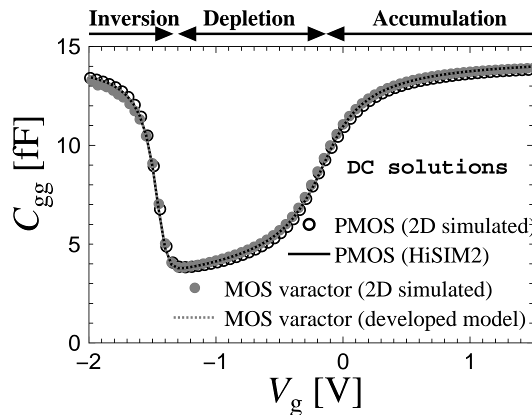

Fig. 2: Studied MOS-varactor and p-channel MOSFET capacitance C_{gg} as a function of V_{gb} or V_{gs} under the DC condition. Symbols show results of the 2D device simulator MEDICI. Lines show results of the developed model.

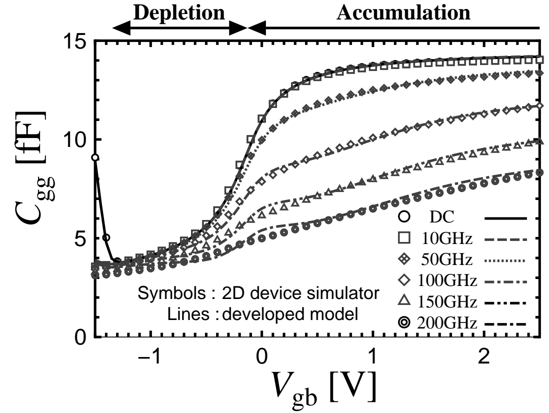

Fig. 3: C_{gg}-V_{gb} characteristic of the studied MOS varactor under AC analysis for different frequencies up to 200GHz. Symbols give the 2D device simulation results, and lines show results with the developed model.

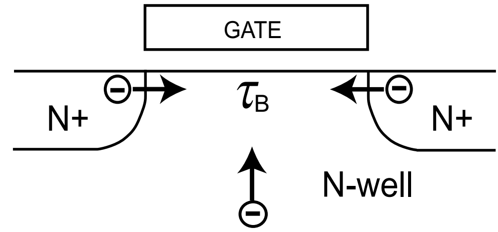

Fig. 4: Concept of the NQS model for bulk carriers. Most of the bulk carriers exist in the two N+ regions. These carriers drift in the channel from/to both sides under the accumulation/depletion condition. Therefore, the majority carrier transit delay τ_B is proportional to the channel length L.

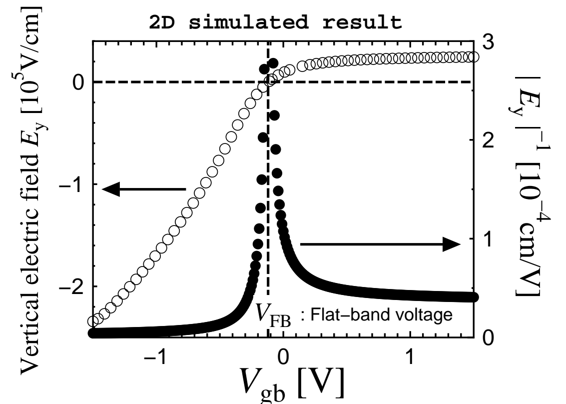

Fig. 5: Vertical component of the electric field 10nm below the middle of the gate oxide as a function of V_{gb}. Positive sign means the field is oriented into the depth direction.

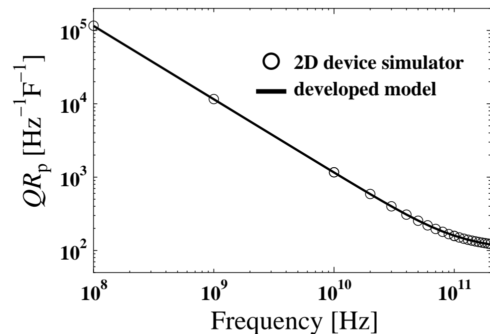

Fig. 6: Quality factor multiplied by the parasitic resistance as a function of frequency at V_{gb}=1V.