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Using MASTAR as a Pre-SPICE Model Generator for Early Technology Assessment and Circuit Simulation

F. Boeuf, M. Sellier, B.Duriez*, E. Josse, A. Pouydebasque*, M.Müller*, F.Payet, B.Borot and T. Skotnicki
frederic.boeuf@st.com; tel : +33 (4) 76 92 55 69 ; fax : + 33 (4) 38 92 29 51, STMicroelectronics, * Philips Semiconductor, 850 rue Jean Monnet, 38920 Crolles Cedex, France

Abstract

In this work we show how to use the MASTAR model in order to generate ready-to-use simple pre-SPICE data. Calibration of MASTAR on silicon data is shown, as well as prediction of device behaviour by architecture changes. The generated pre-SPICE parameters are applied to small circuit simulations such as Ring Oscillator and impact of process dispersion on SRAM functionality.

Introduction

In order to fully evaluate a future technological choice, single device performance is not enough. Indeed in order to monitor the power consumption (e.g. SRAM leakage); speed of a "real-world" circuit (e.g. loaded circuits), and impact of process dispersion on circuit functionality, a System-Level performance evaluation becomes mandatory.

In one hand, the generation of device model for design applications is well known and can be achieved by calibrating full SPICE models on early-silicon data, or by extrapolating models from a technological generation to another. In the other hand, because the fitting parameters are numerous, this approach is extremely time consuming, and difficult to apply to a large range of possible solution (i.e. device architecture change). We propose here a way to rapidly generate pre-sets of data using the MASTAR model, used for the definition of the ITRS Roadmap 2005.This tool can be used by device engineers to be able to get an early evaluation of their devices in circuits, including worst-cases study (dispersion). We will show in a first part that MASTAR model can reproduce silicon data on numerous parameters. In a second part, extrapolation possibility is demonstrated, and finally the example of process dispersion impact evaluation on SRAM cell functionality is given.

Calibration Procedure with MASTAR

Device modelling in MASTAR relies on simple physical equations including Voltage-Doping Transformation [1] for the sub-threshold regime, 1D Airy-function-based quantum calculation for threshold voltage and darkspace corrections, mobility calculation including stress effects, and access resistance calculation based on [2] Moreover, MASTAR can handle FDSOI architecture as well as Double Gate architectures through the use of specific equation-set taking into account both BOX and Silicon thicknesses. In addition, detailed physics module allows computing ballistic correction factor, as well as Si-band structure under stress conditions. The MASTAR model can be found at [4]. Fig. 1 describes how to correctly calibrate MASTAR on silicon-based data. The first step is to describe device geometry and gate stack. The gate leakage improvement factor with respect to SiO_2 is adjusted on silicon data. The second step is to use large width device with various L_{gate}. To determine threshold voltage behaviour on long channel devices both channel doping and gate oxide interface charges can be extracted using the SS and $V_{th,sat}$ values. Next, Both $V_{th,sat}$ roll-off and DIBL(L_{gate}) can be adjusted using junction depth and lateral diffusion factor (Fig. 2), and the pocket model. Once $V_{th,sat}$ and SS are correctly modelled, the off-state current I_{off} can be adjusted : long channel devices allows fitting total junction leakage (e.g. GIDL) and gate leakage level. On short channel, the value of I_{th}=Ids($V_{th,sat}$) can adjusted to match the whole $I_{off}(L_{gate})$ curve (Fig. 3). Saturation regime shall be described using: access resistance Racc, quantum effects in the inversion charge δVth and mobility model. Racc is calculated using the model described in [2]and dVth is using the calculation of the first confined level into a triangular potential E_1, calculated for the nominal channel doping, and such as $\delta Vth=(E_1-kT)/q$. Strain level is modelled through a mobility improvement factor, that may be constant or Lgate dependant (i.e. in the case of a CESL stressor [5]). As a result I_{Dsat}(Lgate) curve can be easily fitted (Fig 4). Finally, Width dependence effects are modelled: Vth,sat(W) is using a VDT description and I_{Dsat}(W) is using model described in [6]), see Fig.5.

Both high-Vth nMOS and pMOS have been successfully modelled using MASTAR. Moreover, lower Vth devices can be extrapolated by only changing the long channel doping, leading to a full model of triple V_{th} platform I_{on}/I_{off} trade—off comparison with silicon is shown in Fig. 6. Using these parameters, devices were generated by reprogramming MASTAR in a BSIM3 model card. As a result both static curves Id-Vd (Fig.7),Id-Vg and Ring Oscillator performance (Fig.8) are comparable to the standard SPICE models.

Predictive Simulation and comparison with Silicon Data

From the previous model, we extrapolated the model to a shrinked MOSFET using thinner gate oxide, lower V_{dd} and modified channel, halos and S/D extension implantations. Only those parameters were modified in MASTAR. The obtained result is in very good agreement with the Silicon data (Fig. 9), showing the predictivity of the tool. Moreover, dynamic performance of a Ring Oscillator was also evaluated and found in good agreement with experimental results (Fig.10)

Dispersion and Corner device generation

Fast, typical and slow devices can be generated from the previous model to be imported into a circuit simulator. Example of worst case variation V_{th}(L) , I_{Dsat}(L). is shown on fig 11. As an example, the simulation of the SNM of a 0.248μm² SRAM cell was performed using various worst cases combinations for Pull-Up, Pull-down and Pass Gate devices. Calculated butterfly curve results are show on Fig. 12.

Conclusion

Using the physics-based MASTAR model with a reduced number of fitting parameters, we show the possibility for device engineers to easily and rapidly generate first-order pre-spice models that can be used in circuit simulator, in order to assess new architecture performances. Moreover, this can be extended to the study of the impact of process dispersion on circuit functionality.

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Reference :
[1] T. Skotnicki et al, Electron Device Letters, Vol 9, N° 3, 1998
[2] S.-D. Kim et al., Trans. Elec. Dev., vol. 49, pp. 457-472, March 2002.
[3] R Gwoziecki et al, Proceeding of ESSDERC 2002, pp 639-642.
[4] available at http://public.itrs.com
[5] F.Payet et al., submitted.
[6] A. Bianchi et al., Proceedings of IEDM 2002, pp 117-120
[7] B. Tavel et al., Proceedings of ESSDERC 2005,pp 423-426.

Step	Device Parameter	Silicon Data	Physics in MASTAR	Model Param.	
1.	Gate leakage improvement / SiO2 Dit, long channel Vth	Jg (Tox,Vg=Vdd) SS(L), D_{it}, $V_{th}(L_{long})$	Tunelling [4] SS(L) VDT model [3]	Oxide IF Jg/Jg^{SiO2} D_{it}, $N_{ch/long}$	Long Channel Devices
2.	DIBL, SCE, SD ext. Overlap, Halos Junction leakage $I_{th}=I_{ds}$(Vg=Vth,sat)	V_{th} (L), DIBL (L) I_{off} (L) I_{off} (L)	VDT [1] - -	Halo dose,energy,specy Xj, SD/gate Overlap(1fp) Ith (1fp), Junction leak (1fp)	Subthreshold Regime short L, wide W
3.	Access Resitance Mobility Strained-Si	- - $I_{dsat}^{Strain}/I_{dsat}^{Unstrain}$ (L)	Based on [2] Universal law Layout dependancy [5]	Device Geometry $K^{\mu}=\mu^{s\text{-}Si}/\mu^{si}$	Saturation Regime short L, wide W
4.	NCE STI Stress along W	Vth(W) Ion(W)	VDT [1] Layout Model [6]	VDT + 1 fitting param. 1 fitting param. [6]	Saturation Regime short L, small W

Fig 1 : Fitting sequence using MASTAR

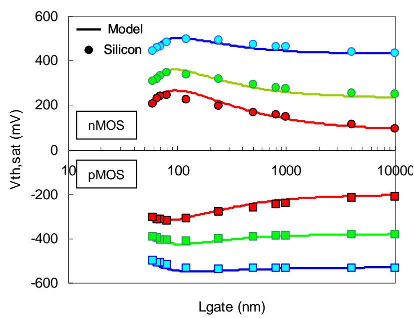
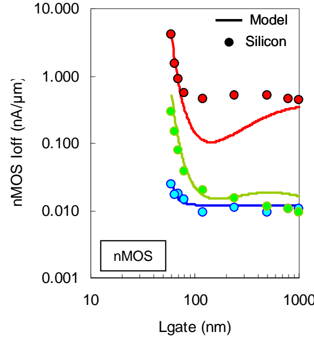


Fig. 2: Silicon vs MASTAR Vth,sat-L comparison for triple Vth platform [7] : blue : HVT, green: SVT and red: LVT



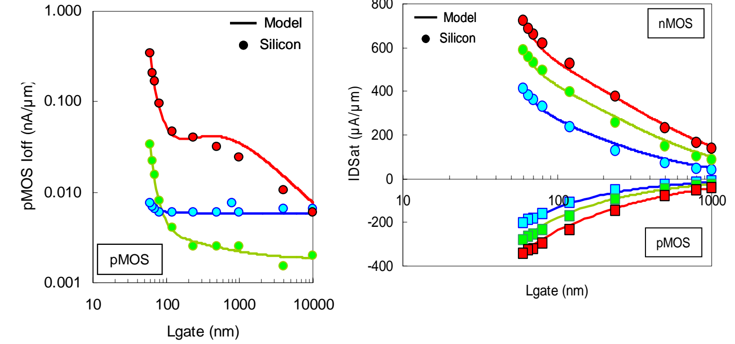


Fig. 3 : Silicon vs MASTAR Ioff. thermionics, gate and junction leakage models are taken into account. : blue : HVT, green: SVT and red: LVT

Fig. 4 : Silicon vs MASTAR IDsat-Width effect comparison . blue : HVT, green: SVT and red: LVT

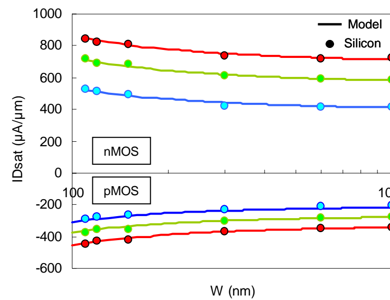


Fig. 5 : Silicon vs MASTAR IDsat-Lgate comparison for triple Vth platform. : blue :HVT, green: SVT and red: LVT

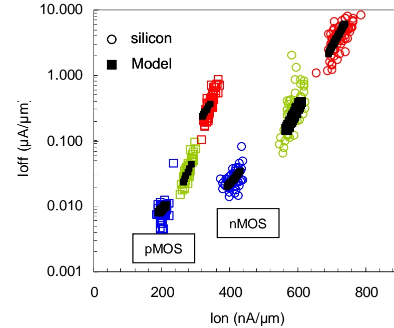


Fig. 6 : Silicon vs MASTAR Ion vs Ioff trade-off for triple vth platform. Strain effects are included in the model.

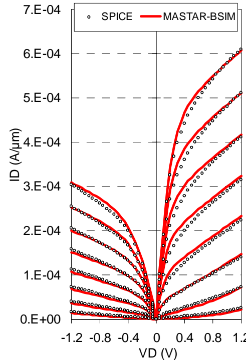


Fig.7: Id-Vd simulation based on MASTAR parameters

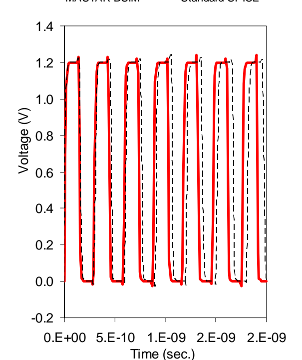


Fig.8: RO FO1 simulation based on MASTAR parameters

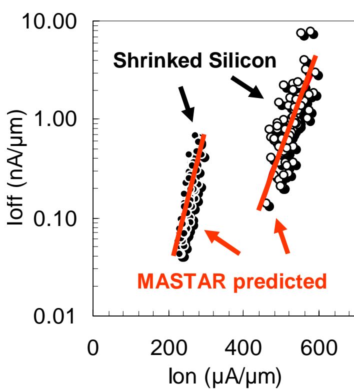


Fig. 9 : MASTAR prediction vs Silicon using architecture changes (Tox, doping of Halo & extensions and Lgate)

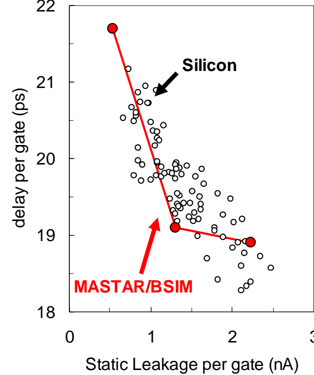


Fig.10 : Predicted vs Silicon Dynamic performances based on MASTAR-BSIM calculation

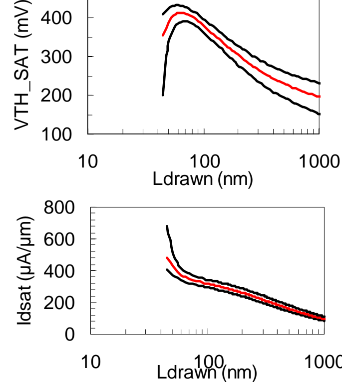


Fig. 11 : Example of worst/best corner cases generated with MASTAR on $V_{th\text{-}sat}$ and I_{Dsat}.for logic devices.

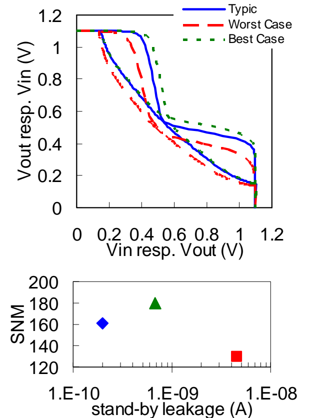


Fig.12 : Example of 0.248µm² SRAM process dispersion study using previously generated corners (matching is not taken into account)