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Strained SiGe-On-Insulator N-MOSFET with Silicon Source/Drain for Drive Current Enhancement

Grace Huiqi Wang, Eng-Huat Toh, Kah-Wee Ang, Chih-Hang Tung*,
Anyan Du*, Yong-Lim Foo†, Guo-Qiang Lo*, Ganesh Samudra, and Yee-Chia Yeo.
Silicon Nano Device Lab., Dept. of Electrical and Computer Engineering, National University of Singapore, Singapore 117576.
*Institute of Microelectronics, 11 Science Park Road, Singapore. †Institute of Materials Research & Engineering, 3 Research Link, Singapore.
Phone: +65 6516-2298, Fax: +65 6779-1103, Email: yeo@ieee.org

1. ABSTRACT

We report the first demonstration of strained-SiGe n-channel field-effect transistors (nFETs) featuring silicon source and drain (S/D) stressors. Silicon S/D, which is lattice-mismatched with respect to the SiGe channel, was employed to induce uniaxial tensile strain in the SiGe channel, leading to enhancement in electron mobility. Device fabrication employed a novel Ge-condensation technique that formed $Si_{0.75}Ge_{0.25}$-On-Insulator (SGOI) substrates with excellent surface quality. Transistors with gate length L_G down to 70 nm were fabricated. At L_G = 70 nm, uniaxial tensile strained-SiGe channel nFETs show 36% higher linear drain current and 20% higher saturation drive current over control SiGe channel devices..

2. INTRODUCTION

Uniaxial strain has been employed to enhance carrier mobility and drive current I_{Dsat} in Si-channel transistors [1]-[2]. SiGe source/drain (S/D) induces compressive strain in Si pFET for hole mobility enhancement [2], and SiC S/D induces tensile strain in Si nFET for electron mobility enhancement [3]. For transistors employing high mobility Group-IV semiconductors/alloys like Ge and SiGe as channel materials, there is little work on channel strain engineering using lattice-mismatched S/D stressors for further mobility enhancement. In this work, we focus on SiGe-on-insulator (SGOI) nFETs and report the first incoporation of Si raised source/drain (RSD) regions to induce uniaxial tensile strain in the SiGe-channel region for I_{Dsat} enhancement. Due to its lattice mismatch with the SiGe, the Si S/D region induces lateral tension and vertical compression in the SiGe channel, leading to electron mobility enhancement.

3. DEVICE FABRICATION

Fig. 1 shows the cross-sections of SGOI nFET device structures fabricated in this work: (a) control SGOI nFET with raised SiGe source/drain, (b) strained SGOI nFET with raised Si S/D regions. 8-inch silicon-on-insulator (SOI) substrates with 35 nm thick Si and (001) surface orientation were used as the starting materials. A strained $Si_{0.88}Ge_{0.12}$ layer with an initial thickness t_i of 73 nm was pseudomorphically grown on each SOI substrate by ultrahigh vacuum chemical vapor deposition (UHV-CVD). A novel cyclic dry thermal oxidation and anneal process was employed for Ge condensation. The cyclic process facilities Ge diffusion, reduces Ge pile-up, and improves compositional uniformity in the SiGe layer. SGOI substrates with Ge content of up to 60% could be formed, as illustrated in Fig. 2.

Fig. 3 summarizes the key process steps used in the device fabrication. As a first demonstration to examine the effectiveness of Si S/D in enhancing I_{Dsat} performance of SGOI nFETs, substrates with 25% Ge were used. In this case, the lattice-mismatch between Si S/D and $Si_{0.75}Ge_{0.25}$ is 1%. A larger lattice-mismatch would promise higher performance enhancement, but could result in dislocation generation. Following active region formation, threshold voltage V_t adjust and well implants were performed. Gate dielectric (EOT ~ 3 nm) was formed by rapid thermal oxidation (RTO). Poly-Si gate electrode material was deposited and patterned. Gate lengths down to 70 nm were achieved. S/D extension implant was performed, followed by 25 nm spacer formation. On one wafer, a selective epitaxial growth of Si(~40nm thick) in the S/D regions was performed [Fig. 1(b)]. On the control wafer, selective epitaxy of $Si_{0.75}Ge_{0.25}$ (~40 nm thick) was performed in S/D regions [Fig. 1(a)]. On both wafers, the S/D regions are raised and are structurally identical. Source/drain implantation and dopant activation (RTA at 950°C for 30 s) followed A TEM cross-section image of a 70 nm gate length SGOI nFET featuring raised Si S/D regions is shown in Fig. 4 (a). The raised Si S/D regions were formed with excellent surface morphology [Fig. 4(b)]. Fig. 5 shows a high resolution TEM (HRTEM) picture of the Si/SiGe heterojunction. A fast Fourier transform diffractogram (inset) on both sides of the heterojunction revealed excellent crystallinity, even after the S/D formation.

4. RESULTS AND DISCUSSION

Taurus-Process simulator was used to study the stress distribution in the $Si_{0.75}Ge_{0.25}$ channel region that arises from the integration of Si S/D regions. Fig. 6 plots the simulated stress profile, showing lateral compression of the SiGe lattice underneath the Si S/D stressors, and lateral tensile strain ε_{xx} in the SiGe channel. Lattice strain analysis was performed using high-resolution transmission electron microscopy (HRTEM) and diffractograms obtained by Fast Fourier Transform of HRTEM sub-images in Fig. 5 [4]. Fig. 7 shows that the lateral strain ε_{xx} is the most compressive in the vicinity of the Si S/D stressor, and decreases with increasing depth. Tensile strain is developed in the SiGe channel, which is key for electron mobility enhancement.

The I_{DS}-V_{DS} characteristics of typical 70 nm gate length transistors with the [110] channel orientation are illustrated in Fig. 8. For the strained SGOI nFET with raised Si S/D regions, a 20% I_{Dsat} enhancement over the control device at a gate over-drive (V_G - V_t) of 1.0 V is achieved. The I_{DS}-V_{GS} characteristics of the devices are shown in Fig. 9. The transconductance G_m of the strained SGOI nFET at V_{DS} = 50mV is 49% higher than that of the control (Fig. 10), indicating mobility enhancement contributed by the Si S/D stressor. Fig. 11 plots the G_m enhancement as a function of gate length. I_{Dsat} enhancement is observed for devices L_G smaller than ~200 nm (Fig. 12). Fig. 13 shows the V_t roll-off for the devices, showing similar DIBL characteristics. Fig. 14 shows that due to larger volume of Si stressor with increasing device width, the drive current as well as strain induced enhancement generally increases. This could be related to the dependence of channel strain on the size of the active region. Fig. 15 examines the dependence of I_{Dsat} on channel direction or orientation. A plan view of device channel direction on the (001) surface is outlined in the inset of Fig. 15. The larger enhancement in the drive current, along [010] channel is attributed to the preferential anisotropic electron population at the 4-fold valley which results in smaller conductivity mass and higher mobility enhancement [5].

5. CONCLUSION

A strained SiGe-on-insulator nFET with Si S/D regions was demonstrated. We demonstrate the first use of lattice-mismatched Si S/D regions as stressors to induce lateral uniaxial tensile strain in the SiGe channel, therefore improving the electron mobility. Substantial I_{Dsat} enhancement was observed. The I_{Dsat} of tensile strained SGOI nFET shows dependency on channel orientations. [010]-oriented nFETs shows the best performance. The use of lattice-mismatched S/D stressors in transistors employing group-IV high mobility channel materials could enable significant speed improvements.

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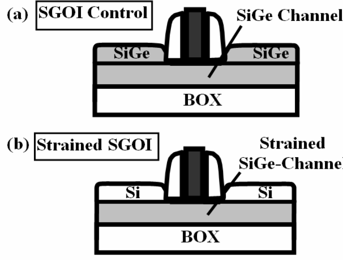

Fig. 1. Schematic of (a) SGOI Control: SiGe channel nFET with Rasied SiGe S/D. (b) Strained SGOI: Strained SiGe channel nFET with Rasied Si S/D.

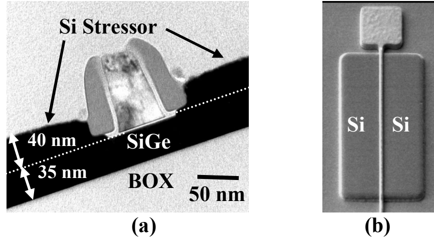

Fig. 4. (a) TEM of Strained SiGe channel transistor featuring Si S/D regions. (b) SEM showing excellent epitaxial quality of Si on SiGe.

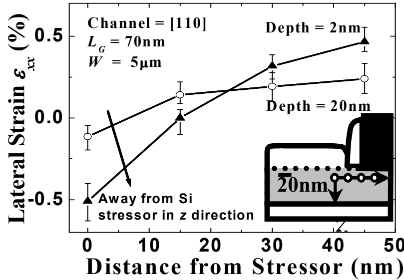

Fig. 7. Strain calculated from reciprocal space diffractogram that is obtained by Fast Fourier Transform (FFT) of HRTEM sub-images.

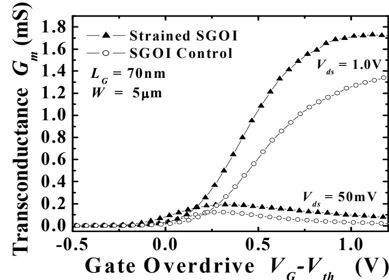

Fig. 10. Transconductance G_m of strained SGOI is enhanced by 31% at V_G-V_{th}=1.0V at V_{DS}=1.0V over SGOI control nFET.

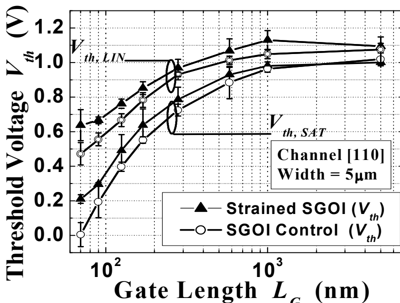

Fig. 13. $V_{th,LIN}$ and $V_{th,SAT}$ for strained SGOI and SGOI control nFET showing similar V_{th} characteristics.

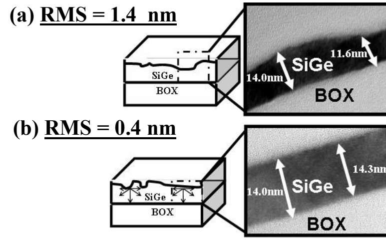

Fig. 2. Schematic process of forming SGOI substrate by Ge Condensation Technique and TEM of SGOI (60% Ge) with (a) oxidation and (b) optimized recurring oxidation and anneal

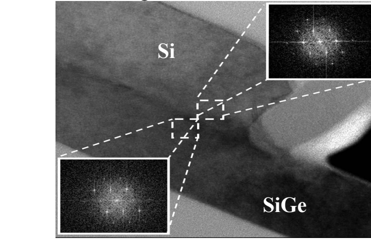

Fig. 5. HRTEM and Fast Fourier Transform (FFT) diffractogram, revealing excellent crystalline quality between Si and SiGe.

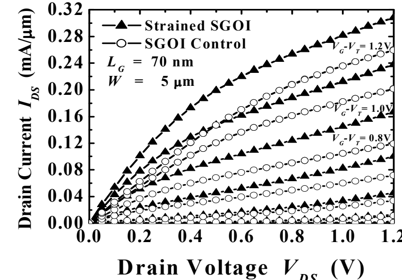

Fig. 8. I_{DS}–V_{DS} characteristics of strained SGOI and SGOI control nFET. I_{Dsat} enhancement of 20% is achieved.

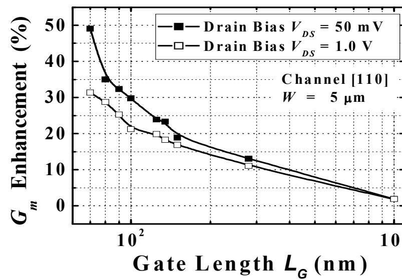

Fig. 11. An enhancement of 49% and 31% is obtained for strained SGOI for G_m at low and high drain bias respectively.

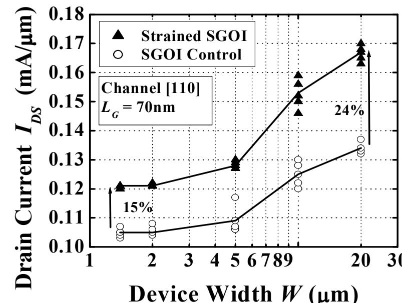

Fig. 14 I_{Dsat} enhancement for strained SGOI at constant gate overdrive of 1.0V shows positive device width dependence.

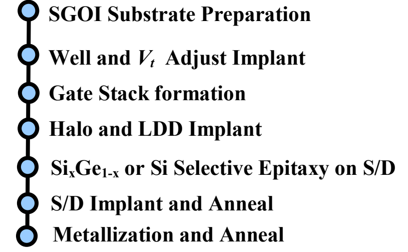

Fig. 3. Overview of process flow sequence. SiGe and Si Selective Epitaxial growth is performed for control SiGe channel and strained SiGe channel nFET, respectively.

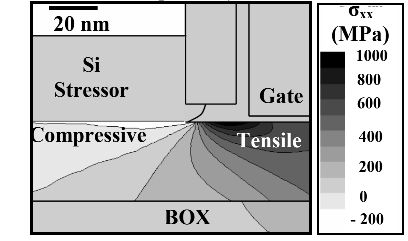

Fig. 6. Process simulation showing compressive strained-$Si_{0.75}Ge_{0.25}$ under the Si stressor and tensile strained-$Si_{0.75}Ge_{0.25}$ in the channel region.

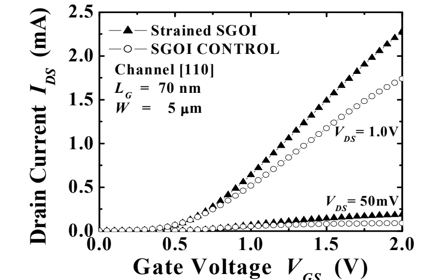

Fig. 9. I_{DS}–V_{GS} characteristics of strained SGOI and SGOI control nFET.

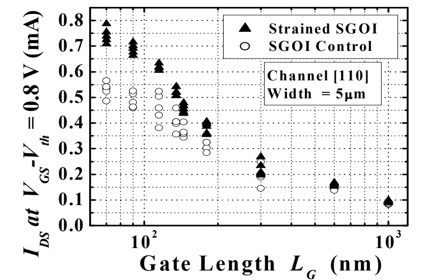

Fig. 12. I_{Dsat} measurement at constant gate overdrive of 0.8V showing significant enhancement for strained SGOI for L_G < 200nm.

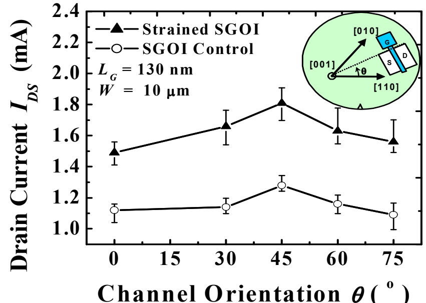

Fig. 15. Highest I_{Dsat} is observed for channel orientation along the <010> direction.