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Ultra-thin Ge-on-Insulator (GOI) Metal S/D p-channel MOSFETs fabricated by low temperature MBE growth

Takashi Uehara, Hiroshi Matsubara, Satoshi Sugahara and Shinichi Takagi
Graduate School of Frontier Science, The Univ. of Tokyo,
7-3-1 Hongo, Bunkyo-ku, Tokyo 113-8656, Japan
Phone & Fax: +81-3- 5841-6733, e-mail: takashi@mosfet.k.u-tokyo.ac.jp

1. Introduction

Scaling of a traditional CMOS is running into fundamental problems, including high leakage current, shallow junction formation, and high parasitic resistance. Thus, new materials and structures are investigated to overcome those problems. As for channel materials, Ge has been expected to replace Si for the future high-speed CMOS technology, because Ge has the much higher carrier mobility than that of Si. However, the water-soluble and unstable germanium native oxides have been the main obstacles to Ge CMOS technology. In addition, smaller bandgap of Ge can cause high source/drain junction leakage current. In order to reduce the leakage current, ultra-thin Ge channel devices have been reported. These devices have used Ge films fabricated by the Ge condensation technique for SiGe epitaxially grown on a SOI wafer by UHVCVD [1], or epitaxial Ge directly grown on a Si wafer by LPCVD [2, 3], as the channels. However, the optimal device structure using Ge channels has not been established yet. Also, the relation of the electrical quality of fabricated Ge channels with structural or fabrication parameters is still unclear. In this paper, we propose and demonstrate a new device structure to exploit the full advantages of high carrier mobility of Ge channels using Ge-On-Insulator (GOI) grown by Low-Temperature Molecular-Beam-Epitaxy (LTMBE).

2. Proposal structure of Ge-on-Insulator (GOI)

In order to solve the above problems regarding Ge MOSFETs, we propose a new GOI MOSFET structure shown in Fig. 1, where metal source/drain is combined with a Si/Ge/Si sandwiched structure, recently reported [4]. This structure holds three advantages. First, the junction leakage current can be reduced by the thin GOI and the increase in E_g due to the quantum confinement. Secondly, this structure can utilize high quality Si/SiO_2 interfaces. Third, using metal source/drain can reduce the parasitic resistance in spite of ultrathin body structure. As the metals for source/drain, we can use, for example, PtGermanide, which is known to have Schottky barrier height lower than 0.1 eV for p-Ge [5]. Fig. 2 shows the schematic band diagram under the inversion condition. Here, Si layers must be thin enough to makes the inversion-layer holes confine only into the Ge channel.

3. Fabrication of Ge-on-Insulator (GOI)

The fabrication steps of the proposed GOI MOSFETs are shown in Fig. 3. In this study, lightly-doped p-type (100) bonding SOI wafers were used for the substrates, where the thickness of the top Si layer and the buried-oxide layer was 100 nm and 50 nm, respectively. First, the SOI thickness was reduced down to 3 nm by thermal oxidation and subsequent etching with BHF. After that, a strained Ge layer was epitaxially grown on the thin SOI, and capped with an 8 nm thick Si cap layer at 100 °C, using molecular beam epitaxy (MBE) (Fig. 3(a)). The thickness of the strained Ge layer was varied from 4 nm to 16 nm. The amount of strain of the Ge layers, evaluated from Raman spectroscopy, was 2.3 % and 1.1 % at the Ge thickness of 4 nm and 12 nm, respectively. Next, post-annealing was performed at temperature ranging from 500 °C to 700 °C for 60 min in forming gas. In order to fabricate Germanide source/drain, a Pt film was deposited by sputtering and patterned by lift-off process (Fig. 3 (b)). A mesa isolation of the GOI layers was done to define the active device area, using reactive ion etching (RIE) in SF_6. PtGermanide regions were formed by annealing at 400 °C for 30 min in a forming gas (Fig. 3 (c)). In order to examine the feasibility of the proposed devices, the Si substrate is used as the back gate and only the back gate operation is evaluated in this study.

4. Results and Discussions

Fig. 4 shows a cross-sectional TEM image of GOI grown by MBE with the Ge layer and the Si cap layer thickness of 12 nm and 8 nm, respectively. The TEM image shows that the bottom and top interfaces of the fabricated Si/Ge/SOI structure are smooth and flat. Fig. 5 shows the V_d-I_d characteristics of the fabricated GOI devices with L/W=100μm/100μm, confirming the transistor operation. Fig. 6 shows V_g-I_d characteristics. It is found that the I_{on}/I_{off} ratio increases with an increase in the annealing temperature, suggesting the recovery of crystal defects by annealing. Fig. 7 shows the annealing temperature dependence of the hole mobility with the Si universal hole mobility for comparison. It is found that the Si/Ge/SOI p-MOSFETs exhibit the highest mobility at the annealing temperature of 600 °C and the value is about 1.5 times as high as the universal mobility, while the mobility decreases at annealing temperatures higher than 600 °C. Fig. 8 shows the Ge thickness dependence of the hole mobility. It is observed that the hole mobility of 4 nm-Ge samples has the lowest value and becomes lower than the universal mobility, while the Ge thickness dependence is small among 8, 12 and 16 nm samples.

In order to examine the dependence of the hole mobility of the annealing temperature and the Ge thickness, physical analyses such as TEM, EDX and Raman spectroscopy are carried out. Fig. 9 shows the results of Energy Dispersive X-ray (EDX) analyses at annealing temperatures of 600 °C and 700 °C, indicating that the inter-diffusion of Si and Ge atoms increases with increasing the annealing temperature. Also, the increase in the interface roughness is observed with increasing the annealing temperature. This fact sug-

gests that the increase in scattering due to the thickness fluctuation [6] is a possible origin of the lowest mobility in the samples with the Ge thickness of 4 nm. Fig. 10 shows the results of Raman spectroscopy. The peak around 400 cm^{-1}, corresponding to the Si-Ge mode in SiGe, increases rapidly at annealing temperatures higher than 600 °C, meaning that Si-Ge bonds are formed at temperatures higher than 600 °C. It was estimated, on the other hand, that the strain of the Ge layers has not significantly changed by the annealing at 700 °C. These results suggest that the mobility decrease by the annealing at temperatures higher than 600 °C is attributable to the formation of SiGe channels caused by inter-diffusion of Si and Ge.

5. Summary

We have proposed and demonstrated a novel ultra-thin Si/Ge/SOI channel structure for GOI MOSFETs. It was found that the fabricated GOI-pMOSFETs have 1.5 times larger hole mobility than the Si universal hole mobility. We have found that the annealing temperature is a significant factor to improve the device quality of Si/Ge/SOI p-MOSFETs grown by LTMBE.

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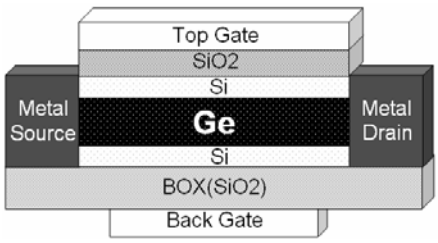


Fig. 1 Cross section of proposed device structure.

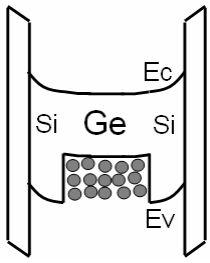


Fig. 2 Band diagram of the proposed GOI structure.

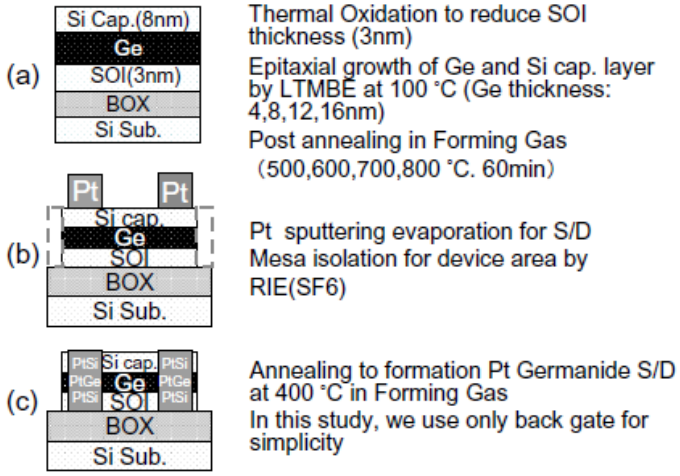


Fig. 3 The fabrication steps of proposed GOI MOSFET.

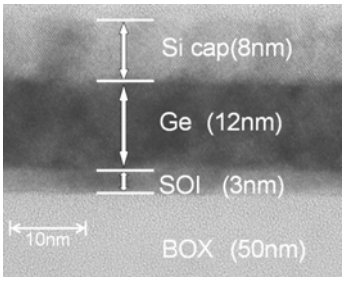


Fig. 4 Cross sectional TEM image of As-grown samples.(12nm-Ge samples)

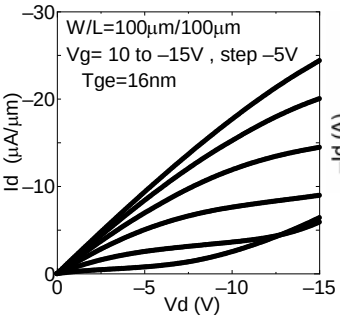


Fig. 5 Vd-Id characteristics of fabricated GOI pMOSFETs. (16nm-Ge samples, annealing at 600 °C)

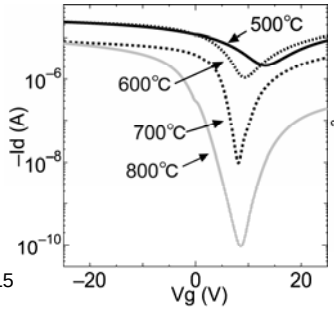


Fig. 6 V_g-I_d characteristics of GOI with the Ge thickness of 16 nm as a parameter of the annealing temperature. The Ion/off ratio increases with increasing the annealing temperature.

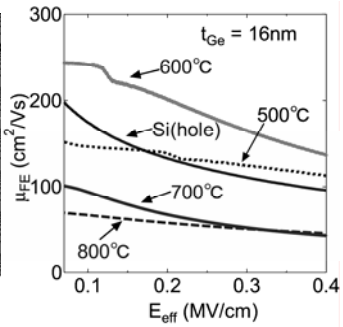


Fig. 7 The annealing temperature dependence of effective hole mobility of fabricated GOI pMOSFETs compared with the Si universal hole mobility. (16nm-Ge samples)

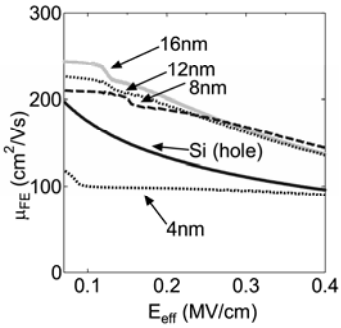
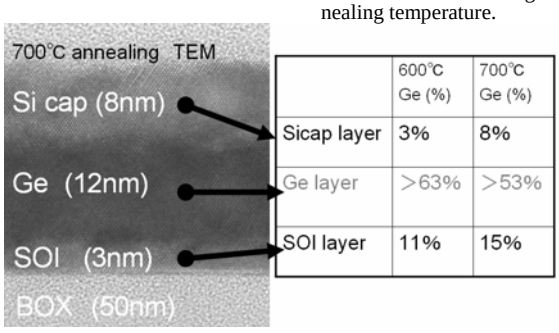


Fig. 8 The Ge thickness dependence of effective hole mobility of fabricated GOI pMOSFETs annealed at 600 °C compared with the Si hole universal mobility.



	600°C Ge (%)	700°C Ge (%)
Sicap layer	3%	8%
Ge layer	>63%	>53%
SOI layer	11%	15%

Fig. 9 Cross sectional TEM image of 700 °C annealing samples with EDX. (12nm-Ge samples). The Ge concentration decreased with a increase in the annealing temperature.

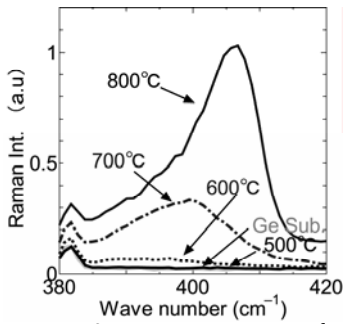


Fig. 10 Raman spectroscopy of fabricated devices with the Ge thickness of 16 nm in comparison with bulk Ge. The peak nearly 400 cm^{-1} indicates Si-Ge in SiGe.