Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Yokohama, 2006, pp. 1052-1053

H-8-3

# Reduction of Parasitic Resistance of Self-Aligned Copper Germanide for Germanium p-MOSFETs

Yu-Lin Chao, and Jason C. S. Woo
Dept. of Electrical Engineering, UCLA, Los Angeles..
420 Westwood Plaza, Los Angeles, CA 90095-1594, USA
Phone: +1-310-206-7331 E-mail: diplodoc@ee.ucla.edu

## 1. Introduction

Recently, germanium has drawn much attention as the high mobility channel materials for future MOSFETs. Up to now, most studies have been focusing on the integration of high-k dielectric gate stack with germanium [1-2]. As devices continue scaling down, however, source/drain parasitic resistance becomes a key limiting factor to the on-current [3]. The performance benefited from the high mobility germanium channel will be diminished if the source/drain region has poor design. To improve the parasitic series resistance, we report the first self-aligned copper germanide germanium p-MOSFETs.

## 2. Experimental Procedures

Individual experiments were carried out on n-type Ge substrates. For Ge MOSCAPs, the gate stack was formed by 1 min 550°C RTO and 2 min 600°C RTN to form a thin germanium oxynitride layer to passivate the germanium surface. 40 Å of LTO was then deposited followed by 600°C RTA for LTO densification and 1000Å Mo gate electrode deposition by an e-beam evaporator.

The study of dopant activation was carried out with boron implantation at 20 keV $4\times10^{15}$ /cm$^2$, or by Ge/B co-implantation with 45 keV Ge implantation energy at a dose of $1\times10^{15}$ /cm$^2$. The activation was performed at 400°C, and dopant concentration was checked with SRP.

Copper germanide was investigated by depositing 500 to 3000Å copper onto HF-cleaned Ge substrates in an e-beam evaporator. Annealing the samples in a nitrogen filled RTA system formed copper germanide at 400°C.

For the self-aligned germanide process, 100Å PECVD oxide and 1000Å nitride were deposited to obtain a bi-layer sidewall, where oxide is used for better film conformity. The sidewall etch process includes an anisotropic dry etch with $CF_4$ gas followed by an isotropic dry etch with $SF_6$ gas and HF dip. The formed sidewall is shown in figure 1.

In device fabrication, regular T-gate structures with width of 10μm and various gate lengths were fabricated on n-type Ge substrates. Field isolation was performed by LTO deposition followed by dry etch to define the active region. A substrate implantation of $7\times10^{12}$ cm$^{-2}$ phosphorous was performed. After gate dielectric deposition, source/drain extension implantation (20 keV, $1\times10^{15}$ /cm$^2$ B), sidewall formation, and source/drain implantation; 500Å of copper was deposited and annealed to form $Cu_3Ge$. After selective wet etch of copper, passivation and metallization were performed.

## 3. Results and Discussions

*Gate Dielectric Technology*

We have previously reported Ge-MOS capacitors with germanium oxynitride/Mo gate stack exhibiting good electrical and material characteristics. [4] For the fabrication of self-aligned germanide MISFETs, however, gate dielectric needs to serve as a reliable etch stop in both gate electrode etch and spacer etch processes in addition to satisfying the electrical requirements. Thus, the devices fabricated in this study uses germanium oxynitride/LTO/Mo gate stack.

The germanium oxnitride/LTO/Mo gate stack has an EOT of 68Å, calculated from the accumulation capacitance in figure 2. The hysteresis is found to be 480mV, much higher than that of germanium oxynitride only gate dielectric (26mV), [4] and is possibly due to long duration of furnace process creating paths for charge trapping. The hysteresis, however, is reduced to 135mV after RTA in mimic of source/drain activation process. The fixed charges in the order of $10^{12}$ /cm$^2$ have also been reduced. Considering the performance of PDA at a higher temperature before Mo deposition, these fixed charges are likely introduced during e-beam evaporation process. The slight drop of EOT after RTA is believed to be a result of increase of germanium oxynitride layer thickness. With the low gate leakage current (figure 3) and other advantages made available by the use of LTO, however, this gate stack allows successful device fabrication and characterization.

*Source/Drain Engineering*

Boron is commonly used as a p-type dopant in group IV semiconductor, and its electrical concentration is usually determined by its solid solubility. The solid solubility of boron in germanium is in the order of $10^{19}$ /cm$^3$, and is much lower than in silicon. Pre-amorphization-implantation (PAI) and solid-phase epitaxial growth, however, can overcome this limitation, [5] and one order higher of activated boron can be obtained as being shown in figure 4.

For the selection of germanide material, we have found that $Cu_3Ge$ yielding excellent electrical properties, with a resistivity of 6.8 μΩ-cm, and a contact resistivity of $8\times10^{-8}$ to $3\times10^{-7}$ ohm-cm$^2$ on p-type Ge. [6] Formation of $Cu_3Ge$ can take place at 400°C, and the high boron concentration achieved by PAI is maintained after germanide formation, as being observed in figure 4. One noteworthy point is that the boron concentration is probed starting at the germanide/Ge interface, and the depth is determined from where the germanide likely ends. It is inconclusive that the higher concentration of boron after germanide formation a result of snow-plowing effect.

*Device Characterization*

The low gate leakage current (<1pA) in the fabricated Ge MISFETs allows accurate device characterization. Illustrated in figure 5 is the transfer I-V characteristic of the fabricated Ge pFETs. The high subthreshold swing is caused by un-optimized isolation and high interface state density. The threshold voltage of the device is extracted to be -1.06V, a result of a high body doping. Figure 6 shows the well-behaved $I_D$-$V_D$ curves of a 5μm gate length transistor. The linearity of the output characteristics at low drain voltage infers good control of parasitic resistance. The carrier mobility is calculated from 10μm gate length transistors using the split CV method, and the mobility is found to be 37 $cm^2$/V-s at an effective field of 0.37 MV/cm. Considering most of the Ge pMOSFETs publications available so far are performed on lightly doped substrate, this mobility is then compared to the silicon hole mobility at the corresponding field and dopant concentration, [7] and is about 40 $cm^2$/V-s. This lower-than-expected mobility in Ge is believed to be the result of the high hysterisis and the high interface state density of germanium oxynitride/LTO/Mo gate stack, and can be improved by other selections of gate stacks. The source/drain parasitic resistance is then extracted from the on-state resistance versus different device gate lengths at identical gate overdrive, (figure 7) and a resistivity of 600 ohm-μm is calculated with a conservative estimation of junction depths. Although this value is still slightly higher than the ITRS requirements, further process optimization of sidewall width and source/drain extension dopant profile can result in lower series resistance, meeting the ITRS specification.

## 4. Conclusions

For the first time, self-aligned copper germanide Ge p-MOSFETs were fabricated and well-behaved I-V characteristics were demonstrated. The source/drain engineering with enhanced electrical dopant concentration and low resistance germanide process were also discussed.


## Acknowledgements

This work is supported by DARPA and MARCO FENA program. The experiments were performed at the UCLA NRF and the UC Berkeley Microlab.


## References


[1] N. Wu, et.al, *IEDM Technical Digest*, (2005) p 563.
[2] S. Whang, et.al, *IEDM Technical Digest*, (2004) p 307.
[3] S.D. Kim, et al. *IEDM Technical Digest*, (2000) p 723.
[4] Y.-L. Chao, et al. SSDM *Extended Abstract*, (2005) p 516.
[5] Y.-L. Chao, et al. *Appl. Phys. Lett.*, 87, (2005) p.142102.
[6] Y.-L. Chao, et al. *IEEE EDL*, to be published.
[7] S. Takagi, et al. *IEDM Technical Digest*, (1988) p 398.


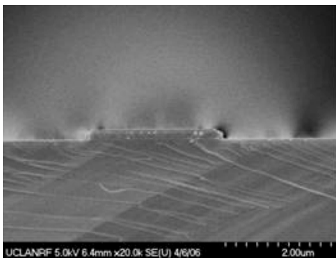


Figure 1 SEM image of the GeON/LTO/Mo gate stack and sidewall.

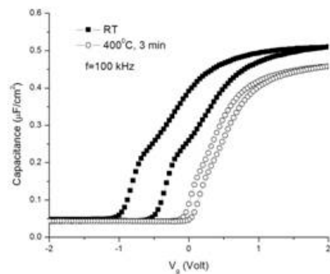


Figure 2 The C-V characteristics of the GeON/LTO/Mo gate stack.

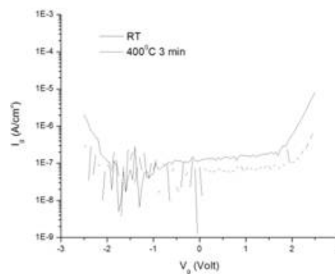


Figure 3 The gate leakage of the GeON/LTO/Mo gate stack.

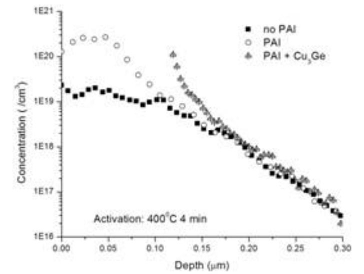


Figure 4 The electrical concentration of boron after RTA and germanide formation.

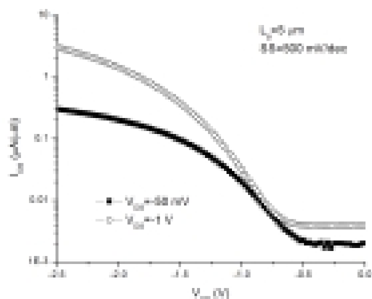

Figure 5 $I_D$-$V_G$ characteristics for the self-aligned $Cu_3Ge$ Ge p-MISFETs.

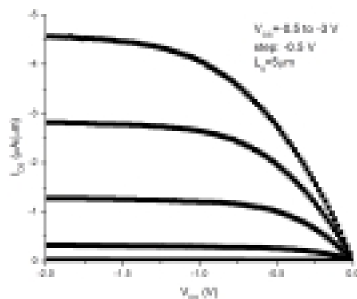

Figure 6 $I_D$-$V_D$ characteristics for the self-aligned $Cu_3Ge$ Ge p-MISFETs.

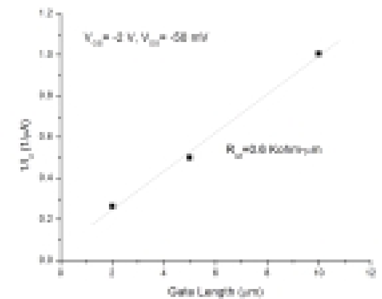


Figure 7 Extraction of the source/drain parasitic resistance for the self-aligned $Cu_3Ge$ Ge p-MISFETs.