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Bendable High-Performance Electronic Devices (Active Transistor, High-Density Interconnect and Passive-MIM Capacitors) on Flexible Organic-Substrate

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1. Abstract

For flexible electronic applications, bendability of electronic devices has been investigated for the first time after devices are transferred onto organic-substrate and wafer thinning. Devices exhibit excellent flexibility and fatigue-resistance (after ~10^3 bending cycles). Devices were pre-fabricated with 0.18 μm CMOS fprocess on bulk-Si and transferred onto flexible FR-4. This suggests a simple way of achieving high performance electronics on flexible through an inorganic/organic hybrid approach without inherent limitation on Si-CMOS processing (materials and temperatures).

Key words: *Bendable integrated circuits, Flexible electronics, Fatigue test.*

2. Introduction

Flexible electronics has attracted a lot of attention for its applications in paper-like display, sensors/actuators, medical devices, RFID, and many others [1-3]. However, it has been a challenge in achieving high-performance transistors on flexible substrates [e.g., 3, 4]. To achieve high performance provided by today's state-of-the-art CMOS technology, wafer level transfer of fully processed active devices from single-crystal Si wafer onto flexible substrate is an attractive approach. Previous studies have focused on structures with μs-Si (and GaAs) [4, 5], pentacene-OTFT [6, 7] and recently with CMOS devices fabricated on Epi over porous-Si [8].

One of the natural concerns for such an approach would be mechanical tolerances (i.e., bending tolerance and fatigue characteristics upon repeated bending) of the transferred single-crystal Si-based devices. In this work, we have demonstrated successful transfer (onto an organic-substrate) and thinning of bulk Si with MOSFET, passive MIM-capacitors and high-density interconnect. The transferred devices exhibit excellent mechanical tolerance; i.e., functional for bending up to radius ~126mm, and no failure seen up to ~10^3 bends. These suggest the feasibility of utilizing high-performance devices hybridized with organic components in future large area flexible yet performance sensitive products.

3. Experiments and Results

The active transistor, MIM capacitor and high density Cu/low-κ (Black Diamond ^{TM}) based interconnect with 0.18μm design rule were fabricated on bulk-Si wafers (p-type, ρ~10Ω·cm). The fabrication is followed by the wafer-transfer-technology [9]. The flatness and bendability of the transferred and thinned wafer can be seen in Fig. 1(a). Cross-sections of the transistor and Cu/low-κ interconnect on FR-4 were shown in Fig. 1(b). The active transistors, Cu/Low-κ interconnect and MIM capacitors were characterized by Agilent-4156C**,** HP-34401A multi-meter and HP4284A impedance analyzer, respectively. The bending test setup is shown in Fig. 2.

The transistor characteristics (L=0.17μm) in both bending directions (compressive and tensile, with radius ~±72mm) are shown in Fig.3-4. The threshold voltage (V_{th}) and subthreshold slope (SS) are insensitive to the bending, but the drive-current (I_{ds}) illustrates the strain effect upon such bending (Fig.4). To study the strain effect, the Raman spectrums were measured on the backside Si of active transistor under each bending condition (Fig.5). In Si, the compressive and tensile strains were generated by bending the substrate upward and downward, respectively, as detected by the peak's shift of Raman spectrum [10]. Those strains modulate the transistors performance by changing the band structure [11], thus increases or decreases I_{ds} as the substrate being bent upward or downward. After bending release, the Si Raman peak shifts back to original, indicating that the deformation within the thinned wafer is recoverable.

The fatigue test was conducted by bending the wafer in sequence of upward, release to flat, downward and release to flat cyclically. And we chose a less bent condition (radius~±126mm). *There is no discernable degradation of transistors' performance by examining the curves of I_D-V_G, I_D-V_D and g_m after ~10^3 bending cycles* as shown in Fig. 6-7.

The impact on via-chain (size/number: 0.26-0.5μm/~10^4 vias) performance from different bending and fatigue cyclical test is shown in Fig. 8-9, *negligible change was seen (≤5%).*

Similar bending test was applied on the MIM capacitors. The capacitance modulation with bending radius is negligible also, as shown in Fig.10, and the *maximum variation in bending cyclical test (~10^3) is within ±0.5%* (Fig.11). This is different from organic-based capacitors [6]: the capacitance modulates with degree of bending, ~4% was observed.

4. Conclusion

We have demonstrated successful transfer of devices fabricated through standard CMOS process onto organic-substrates for flexible electronics application. The characteristics of transistors, MIM-capacitors and high-density interconnect are not affected by the bending applied to the flexible organic-substrates suggesting the feasibility of achieving high performance electronics on flexible substrates.

References

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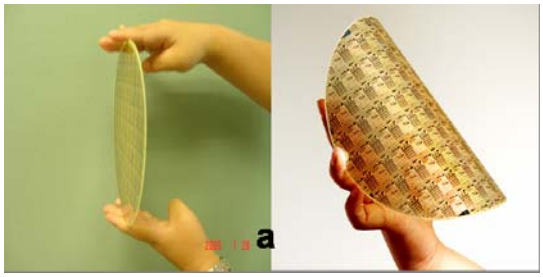

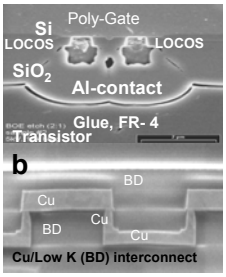

Fig.1. The devices on the FR-4 (4 mils) after WTT (a) The cross-section of transistor and Cu/Low K (BD) interconnect on flexible organic-substrate(FR-4) (b).

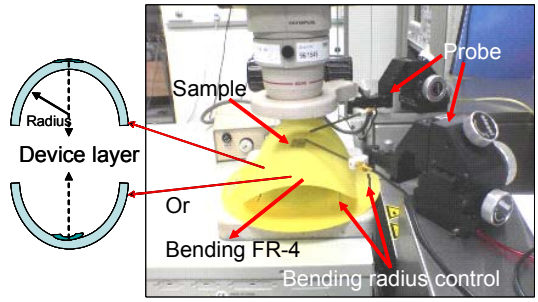

Fig.2 The setup of bending test.

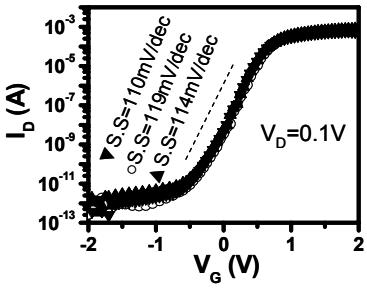

Fig.3 Id-Vg characteristics of active transistor (W/L=10μm/0.17μm) on upward and downward bending substrate. upward bending (▼radius:-72mm) downward bending (▲radius: 72mm) and flat (○) status.

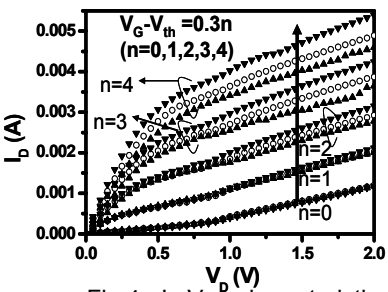

Fig.4 I_D-V_G characteristics of active transistor with W/L (W/L=10μm/0.17μm) on upward bending (▼radius:-72mm) downward bending (▲radius: 72mm) and flat (○) status.

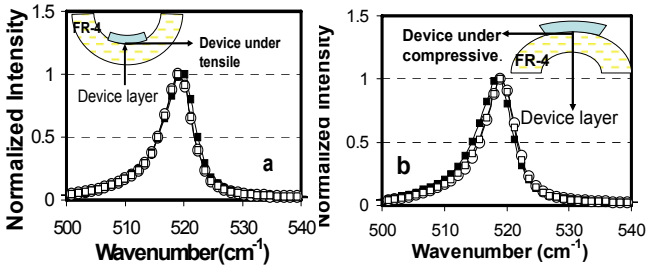

Fig.5 Raman spectrum of bulk Si upward (a) and downward (b) at the flat(○), bending(■ radius 72mm) and release bending (□) status.

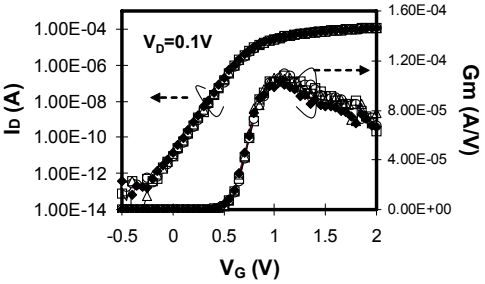

Fig.6 I_D-V_G and Gm characteristics of active transistor with W/L(1.4/0.18μm) at different bending cycles times. (○: before bending, □:bending cycle 3, Δ:bending cycle 10, ♦: bending cycle 1000).

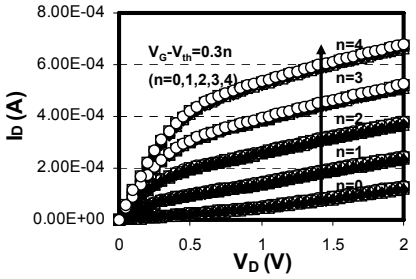

Fig.7 I_D-V_D characteristics of active transistor with W/L(1.4/0.18μm) at different bending cycles times. (○: before bending, □:bending cycle 3, Δ:bending cycle 10, ♦: bending cycle 1000)

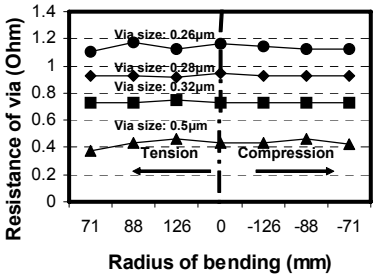

Fig.8 The via resistances with different via sizes (via number:11182) at different bending radius.

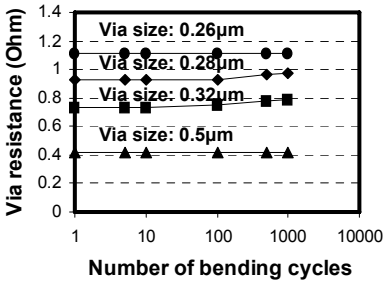

Fig.9 The via resistances for different via sizes (via number:11182) at different bending cycles test.

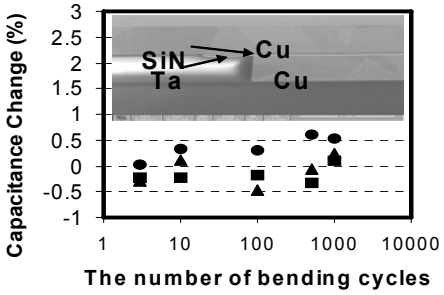

Fig.10 The capacitances at different bending cycles measured that capacitors with different plate area. Square plate length: (● 109.5μm, ■ 54.8 μm and ▲44.7 μm.)

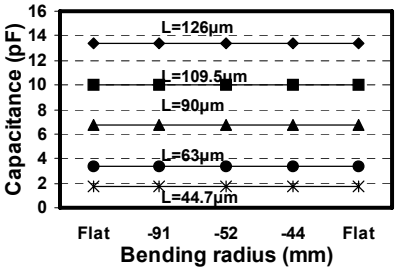

Fig.11 Capacitances of capacitors with different square lengths at different upward bending radius.