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Comparative Study on Influence of Subband Structures on Electrical Characteristics of III-V Semiconductor, Ge and Si Channel n-MISFETs

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1. Introduction

Several physical limitations on device scaling strongly demand continuous enhancement of carrier transport properties in MOS channels with progression in the technology node. Thus, a variety of new channel structures and materials have been intensively developed. In p-channel MOSFETs, particularly, many device concepts such as (110) surfaces, uni-axial compressive strain and Ge channels have already been proposed and demonstrated. As for n-channel MOSFETs, however, there have currently been few promising device concepts since the introduction of the tensily-strained channels.

It is well known, on the other hand, that III-V compound semiconductors can provide quite high electron mobility, as shown in Table 1. Thus, the application of III-V MISFETs to the Si platform has recently stirred a strong interest. Actually, the detailed analyses have recently been reported for double gate MOSFETs using III-V channels [1, 2]. However, the electrical characteristics of III-V channel scaled n-MISFETs, in particular bulk MISFETs [3], have not been fully studied yet. Here, one of the most important issues on the understanding of the electrical characteristics of scaled MISFETs with ultrathin gate oxides is the influence of the subband structures, which are significantly different among III-V, Si and Ge. Thus, this study theoretically examines the device performance of bulk III-V MISFETs in comparison with those of Si and Ge ones from the viewpoint of the subband structures.

2. Calculation Model

The calculations are carried out for bulk Si, Ge, GaAs, InP, InAs and InSb MISFETs on (100) surfaces and Ge on a (111) surface. We have already reported that the (111) Ge MISFETs can provide better performance than (100) [4, 5]. The substrate impurity concentration, N_{sub} , is fixed at $1 \times 10^{18} \text{ cm}^{-3}$ for being applied to short-channel bulk MISFETs. The valleys and the values of the effective mass [3] used in the calculations are shown in Table 1. It should be noted here that the III-V materials has the L valleys with higher effective mass and resulting lower mobility than the Γ valley. Thus, the energy difference between Γ and L valleys, $\Delta E_{\Gamma L}$, is an important physical parameter to determine the population of electrons in the L valleys. The subband structure is determined by the self-consistent calculations for Poisson and Schrodinger equations. The drain saturation current under ballistic transport, I_{on} , calculated by the formulation of Natori [6], is used for estimating the current drive of each MISFET. The current flow direction is taken to be parallel to <110>.

3. Results

It is found that two factors associated with the subband

structures of the III-V materials can degrade I_{on} . One is the transfer of electrons into the L valleys with higher effective mass, which has been reported for the ultrathin body double gate devices [2], and the other is the lower inversion-layer capacitance, C_{inv} , and resulting lower equivalent gate oxide thickness, T_{eq} [3]. Fig. 1 shows the electron occupation in the Γ and the L valleys as a function of surface carrier concentration, N_s . It is found that InP and InAs have no electron occupancy in the L valleys, while more electrons in GaAs and InSb MIS occupy the L valleys with an increase in N_s , because of the smaller $\Delta E_{\Gamma L}$. This occupation of the L valleys in GaAs and InSb can lead to the lower I_{on} due to much higher effective mass of the L valley electrons. Fig. 2 shows the increase in T_{eq} due to C_{inv} . It is found that ΔT_{eq} is much thicker in the III-V materials, because the lower effective mass causes the decrease in the density-of-states and the thicker inversion layers [7], both of which increase C_{inv} . This thicker T_{eq} can seriously affect I_{on} , because the increase in T_{eq} reduces N_s at a given V_g and the resulting I_{on} . Also, the decrease in ΔT_{eq} of GaAs and InSb seen in high N_s region, attributed to the electron transfer into the L valleys. Although lower N_{sub} can lead to the reduction in the transfer into the L valleys in GaAs, this accompanies the increase in ΔT_{eq} (Fig. 3).

On the other hand, the injection velocity, v_{inj} , at the source edge and resulting I_{on} under the ballistic transport, shown in Fig. 4 and 5, respectively, are found to be significantly enhanced in the III-V MISFETs at a fixed N_s , attributed simply to the lower effective mass. The decrease in v_{inj} of GaAs and InSb in high N_s region is caused by the electron transfer into the L valleys, shown in Fig. 1, which is similar with the velocity-electric field curves. The above results mean that the effective mass of MIS channel materials can provide the trade-off relationship between v_{inj} and N_s at a fixed T_{ox} and V_g [5]. Thus, the optimum channel material in terms of I_{on} ($=qN_s v_{\text{inj}}$) at a fixed V_g can depend on T_{ox} , because C_{inv} reduces gate capacitance more with thinner T_{ox} . Figs. 7-9 show the $I_{\text{on}}-V_g$ curves with T_{ox} of 3, 1.5 and 0.5 nm, respectively. Here, I_{off} at V_g of 0 V is fixed at $0.3 \mu\text{A}/\mu\text{m}$. It is found in the results with T_{ox} of 3 nm that the III-V materials provide higher I_{on} than Si and Ge. The saturation of I_{on} in GaAs is attributed to the electron transfer of the L valleys. Also, lower I_{on} in InSb seen in low V_g region and in the other T_{ox} is due to the very thick T_{eq} , shown in Fig. 2. In thinner T_{ox} , however, the superiority of the III-V channels becomes smaller. It is found in T_{ox} of 0.5 nm that I_{on} in the III-V channels is comparable to that in Si and lower than that in (111) Ge, attributed to the increased contribution of thicker T_{eq} . Thus, ultrathin-body III-V channels are expected to improve the performance, because

the inversion-layer thickness is reduced down to the body thickness. Among the III-V channels, InP and InAs in thicker T_{ox} seem to provide the higher performance. As a consequence, while the III-V materials, in addition to (111) Ge, are promising channels, the advantage is more evident in T_{ox} thicker than 1.5 nm.

4. Conclusion

It has been found that the lower effective mass of the III-V MIS channels can provide higher velocity, while it significantly reduces C_{inv} and increase in T_{eq} , resulting in lower N_s at a given V_g . Thus, higher performance is expected in III-V MISFETs with thicker T_{ox} , typically

	Si	Ge	GaAs	InP	InAs	InSb
electron mob. (cm^2/Vs)	1600	3900	9200	5400	40000	77000
mass (Γ)			0.063	0.082	0.031	0.0118
mass (Δ)	mt	0.19	0.2			
	ml	0.916	0.95			
mass (L)	mt		0.082	0.127	0.153	0.124
	ml		1.64	1.538	1.878	1.565
$\Delta E_{\Gamma L}, \Delta E_{LA}$ (eV)		0.15	0.447	1.492	1.607	1.03
Eg (eV)	1.12	0.66	1.42	1.34	0.36	0.17

Table 1 Effective mass and the other band parameters of the conduction bands for Si, Ge, GaAs, InP, InAs and InSb [3]

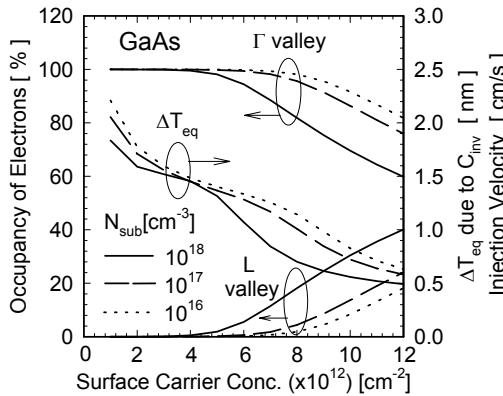


Fig.3 Electron occupancy and increase in T_{eq} of GaAs with different N_{sub} as a parameter of N_s

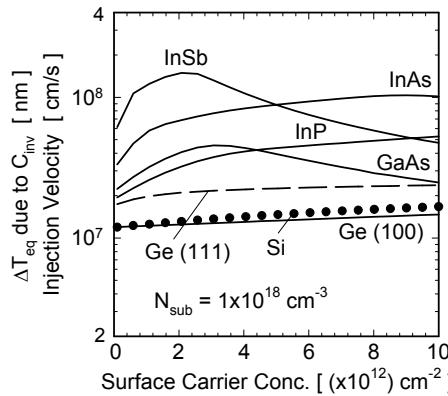


Fig.4 Injection velocity at the source edge as a function of N_s

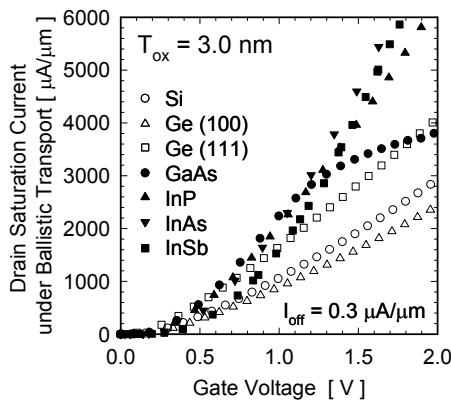


Fig.6 I_{on} under the ballistic transport versus V_g with T_{ox} of 3.0 nm

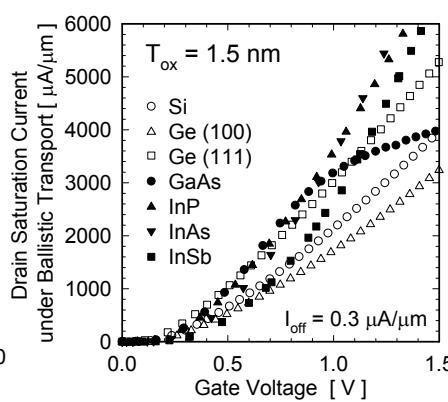


Fig.7 I_{on} under the ballistic transport versus V_g with T_{ox} of 1.5 nm

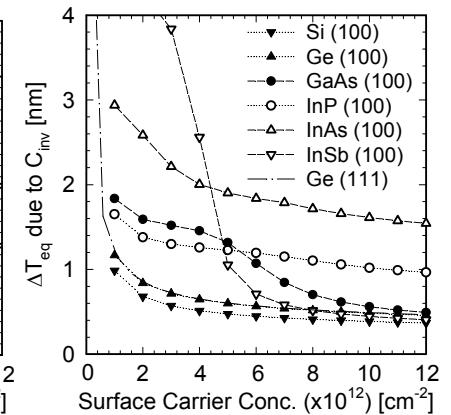


Fig.1 Electron occupancy of III-V channels in Γ and L valleys as a function of N_s

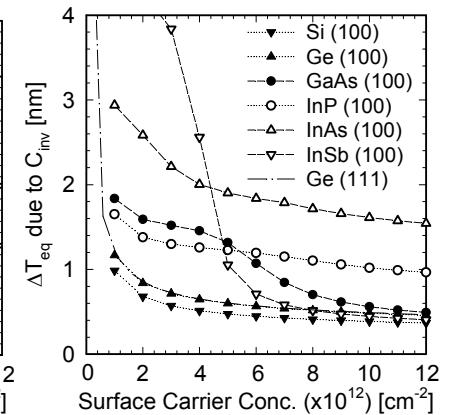


Fig.2 Increase in equivalent gate oxide thickness due to C_{inv} as a function of N_s

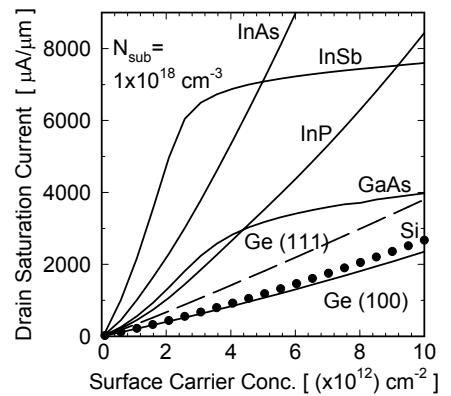


Fig.5 I_{on} under ballistic transport with N_{sub} of $1 \times 10^{18} \text{ cm}^{-3}$ as a function of N_s

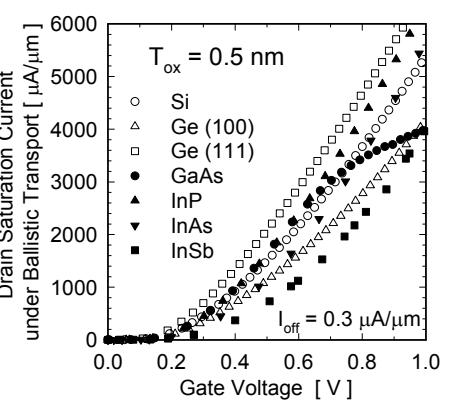


Fig.8 I_{on} under the ballistic transport versus V_g with T_{ox} of 0.5 nm

thicker than 1.5 nm. InP and InAs MISFETs can yield higher I_{on} than GaAs and InSb ones, because of no electron transfer into the L valleys due to larger $\Delta E_{\Gamma L}$. The ultrathin-body channels are expected to further improve I_{on} .

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References [1] A. Rahman et al., IEDM (2005) 615 [2] A. Pethe et al., IEDM (2005) 619 [3] M. Fischedi, TED-38 (1991) 634 [4] S. Takagi, VLSI symp. (2003) 115 [5] S. Takagi, SSDM (2004) 10 [6] K. Natori, IEICE Trans. Electron., E84-C (2001) 1029 [7] S. Takagi et al., TED-42 (1995) 2125