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A Practical, Systematic, Simple Method to Evaluate Speed/Bandwidth Potential of CMOS Processes for Analog Design and Related Practical Considerations

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1. Introduction

Estimation of maximum clocking rate of a given process for digital applications is fairly simple to determine. It is set by inverter gate delay. However, the situation is not as simple for analog applications. It is clear that bandwidth depends on constraints set by power consumption, signal swing, linearity, load capacitance, etc. Since this dependence is not a very straight forward one, and there is a thirst for higher speed in many of today's applications, inexperienced designers can fall in a design loop unless they have a clear estimate of what is achievable by given process. In other words knowing the limit for bandwidth, given a process, is of prime importance and can save considerable amount of design time for analog designers. Here we first show drawbacks of conventional transit time frequency. Second, we provide a practical simulation circuit to estimate device cut off frequency. Third, we present a systematic method to estimate bandwidth and/or speed, achievable by a given process, based on estimated device cut off frequency. This is especially useful to avoid the loop of increasing bias currents, modifying phase margin, and again increasing bias currents, .in pursuit of higher bandwidth in feedback circuits.

2. Device Transit Frequency

Conventional Method

Figure 1 shows the circuit diagram conventionally used to estimate transit frequency f_T of an MOS device. It is based on what is done for bipolar devices. However, there are quite a few practical difficulties or shortcomings. First, in practice never a current signal is fed to the gate of an MOS device. Second, for simulation there must be a bias circuit. Third, the bias circuit, a voltage source in series with a resistor placed in parallel to the current source, creates an extra pole which can confuse an inexperienced designer especially when a small resistor value is selected. Last it does not take into account body effect which reduces bandwidth in often used cascade circuits.

Practical Method

Figure 2 shows the circuit diagram for estimating MOS device cut-off frequency realistically while keeping the circuit very simple. The bias voltage here does not add any extra pole, as in the conventional method [1]. The diagram was drawn from the fact that very often in analog CMOS circuits cascode structures are needed to boost dc gain. We purposely have kept sizes of the MOS devices equal, and their source and drains (at the cascade node)

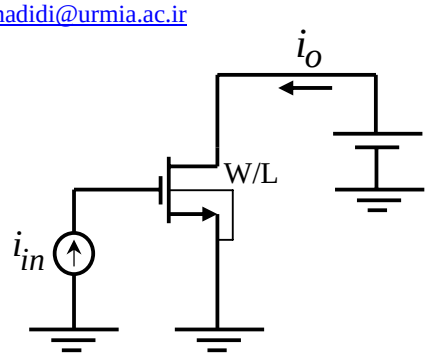

Fig. 1 Conventional circuit to evaluate MOS transit frequency

separate to take into account more accurately parasitic capacitors without making the circuit complex. Notice that the diffusion areas for simulation should be considered based on layout design rules to accurately include parasitic capacitances. Furthermore, in sharp contrast to the circuit of Figure 1, here naturally body effect of the cascade device affects the outcome as in real analog blocks. Now a simple AC simulation reveals -3dB bandwidth of the output current, which we call "device' cut-off frequency". Notice that in cascode OTAs, perhaps the most common circuit in analog applications, device cut-off frequency determines the cascode node bandwidth. If a PMOS design, for any reason preferred, then with a similar diagram/simulation, cut-off frequency for PMOS devices is obtained. The cut-off frequency is then can be used to estimate the achievable process bandwidth.

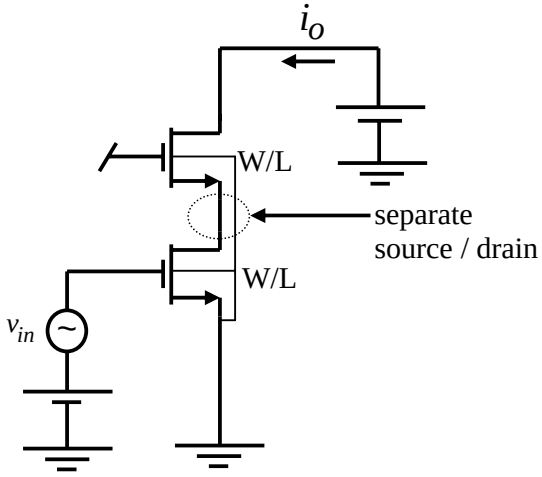

Fig. 2 Proposed circuit to evaluate MOS cut-off frequency

3. Unity-Gain Frequency and Achievable Bandwidth

The cut-off frequency f_{co} imposes an upper limit on unity gain frequency in analog circuits given a specific process. However, bandwidth is further limited due to other reasons. Feedback is employed very often in analog applications, such as accurate gain stages, OTAs, PGA/VGAs, etc. Indeed here the cut-off frequency determines the second pole frequency. For feedback loop be stable with a satisfactory phase margin φ_m, the unity gain frequency is further limited. Figure 3 shows open loop frequency response of a folded cascade OTA. Considering a 70 degrees phase margin, the unity-gain frequncy f_u becomes $f_{co}/\tan\varphi_m$. This is an upper limit in feedback circuits. However, it is a well known fact that feedback is used for two main reasons a) to achieve a fixed gain, or rather a relatively fixed gain, and b) to achieve high linearity. Both of these require a loop gain much larger than 1 at the desired frequency of operation. As a rule of thumb we can consider the highest frequency for desired operation where the loop gain remains more than 10. Thus, upper frequency limit in a given process becomes $f_{bw} = f_{co}/27.5$ for a loop gain of 10. Notice that when signal swing is small and/or demand for linearity is limited, then a much smaller loop-gain, say 5 or 3, might be acceptable at the maximum frequency of operation. Then achievable bandwidth will be many times higher.

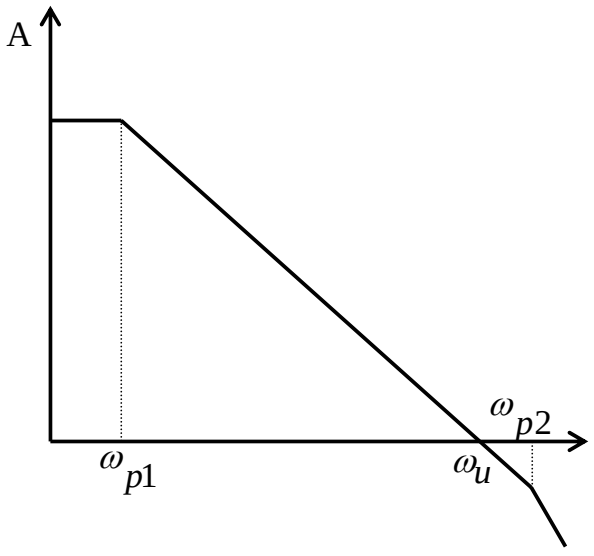

Fig. 3 Frequency response of a folded cascade op-amp

4. Practical Considerations

In estimation of process bandwidth we did not specify overdrive voltage, which inversely affects transconductance, dc gain, and bandwidth. Depending on the overdrive voltage considered, the process bandwidth will vary if no other effect is taken into account. However, an important parameter which must be considered in analog designs is the required linearity. For a given signal swing linearity enhances as overdrive voltage of the driving device increases. Specifically, in differential circuits, for a given signal swing, linearity enhances in proportion to square of overdrive voltage. Hence one must balance these two conflicting requirements. Since an overdrive voltage of 0.15 volt delivers the highest efficiency $f_T g_m/I_d$ [2], in many of leading CMOS processes, from 0.35um to 0.18um, we suggest a 0.15 volt overdrive voltage be set by adjusting the bias voltage in simulation of Fig. 3. This would reveal a circuit with optimum use of power. Moreover, since V_{ds} affects transconductance as well as cut-off frequency of a device with a specific size and bias current, there is a trade off between output voltage swing, linearity and V_{ds} of the cascaded devices. We suggest a V_{ds} of 0.3 to 0.4 volt as a reasonable compromise considering all important performance parameters. It can be shown that if power is constrained in branches of a folded cascade op-amp, for a given signal swing different values of overdrive voltages does not much affect the maximum bandwidth for a given linearity. While when there is no power constraint, the outcome will be different in each case.

5. Some Simulation Results

Table 1 shows estimated cut-off, unity-gain, and loop-gain-of-10 bandwidths for 0.18um and 0.35um CMOS processes. Notice that depending on the output signal range and linearity required one might find achievable bandwidth many times higher than f_{bw} in table below up to f_u.

Table 1 *fco* and *fu* of 0.35 μm and 0.18 μm processes

	0.35 μm Vov=0.15V Vds=0.4V	0.35 μm Vov=0.20V Vds=0.4V	0.18 μm Vov=0.15V Vds=0.3V	0.18 μm Vov=0.20V Vds=0.35V
f_{co}	6.7GHz	8.4GHz	24.6GHz	31.6GHz
f_u	2.4GHz	3.1GHz	9GHZ	11.5GHz
f_{bw}	240MHz	310MHz	900MHz	1.15GHz

6. Conclusions

A simple practical method to estimate CMOS processes bandwidth for analog applications was presented. Using the method the process "cut-off" frequency, as well as achievable bandwidth in feedback circuits are accurately estimated. Also, practical considerations regarding V_{ds} and overdrive voltages were discussed. Slides of oral presentation, including further detailed treatment are available through contacting author.

References

[1] Kh. Hadidi, Course Notes on Analog CMOS Design, Urmia University.

[2] Y. Taur and T.H. Ning, Fundamentals of Modern VLSI Devices, Cambridge University Press, 1998.