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Low-Voltage, Low-Phase-Noise Ring-VCO using 1/f-Noise Reduction Techniques

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1. Introduction

The challenge in the design of a fully integrated CMOS phase-locked loop (PLL) for a wireless data transmission network is to achieve a low-voltage operation, a low phase-noise and a wide frequency range. A ring oscillator is attractive to implement a compact on-chip voltage controlled oscillator (VCO), however its phase-noise is larger than an LC VCO because it is affected by 1/f noise in a MOSFET.

In this paper, a ring-VCO utilizing 1/f-noise reduction techniques and its application to a PLL are described. Due to the proposed techniques, which use a MOSFET current-source operated in a triode region and a switched bias circuit, phase noise of the VCO and PLL is decreased.

2. 1/f Noise Reduction Technique for VCO

In modern submicron CMOS process, 1/f noise is a critical noise source and it is important issue from a perspective of phase-noise. The 1/f-noise source in a MOSFET operated in the saturation region is a trapping and de-trapping of carrier in the gate oxide. Thus a switching MOSFET technique that compulsorily de-trap the trapped career have been reported for 1/f-noise reduction techniques [1-2]. Furthermore, it is necessary to design a ring-VCO using a MOSFET operated in the triode region in order to reduce the 1/f noise.

3. Circuit Design

The schematic of a ring-VCO delay cell is shown in Fig. 1. The current sources are placed with both edges, and its control current consumption in CMOS inverter. The both current source are implemented by 6-selector-switches and 6-MOSFETs of MP1 to MP3 and MN1 to MN3 operated in the triode region. Due to the triode region operation, the 1/f noise of the current source is reduced. The current source operated in the triode region suppresses the operating frequency range of the ring VCO because of a low transconductance gm, however the selector switches extend the operating frequency range.

The schematic of a switched bias-circuit (SBC) is shown in Fig. 2. It consists of 2 level-shifters and 2 identically bias-branches that are used alternately with only one-sided “ON” at any time. The unused bias branch is switched off by the CK signal. As a result, a trapping carrier in the gate oxide is de-trapped and the 1/f noise is reduced. Owing to the switching operation, the proposed bias-circuit suppresses an increase of power consumption.

The block diagram of PLL is shown in Fig. 3. The PLL consists of a ring-VCO with SBC, a phase-frequency detector (PFD), a low pass filter (LPF) and a prescaler (DIV). The LPF was implemented in off-chip discrete devices.

4. Experimental results

A chip micrograph of the PLL fabricated with a 0.18-μm CMOS process is shown in Fig. 4. Figure 5 shows the measured oscillation frequency of the ring VCO versus the control bias voltage Vcn and Vcp. The ring VCO has a low VCO-gain of 500-MHz/V, however the selector switches extend the operating frequency range from 500-MHz to 1.2 GHz. The ring VCO achieved a 1.0-GHz oscillation and a 710-μW power dissipation at 1-V supply.

The measured phase noise of the ring VCO at 100-kHz offset versus the control bias voltage Vcn and Vcp is shown in Fig. 6. The minimum values of the phase noise are observed in the triode region, and it is improved by about 7 dB. The measured phase noise curves of the ring-VCO with and without switched biasing for 1-GHz output is shown in Fig. 7. The SBC was operated at a 10-MHz clock. The SBC reduced the phase noise by 3-dB and the ring VCO achieved -68-dBc/Hz at 100-kHz offset.

The performance comparison of referred PLLs and the measured PLL using the proposed ring VCO is summarized in Table 1. Usually, a phase-noise figure of merit (FOM) is as follows:

$$FOM = L+10\log[(\Delta f/fosc)^2 (P/1mW)] \quad (1)$$

where L is the phase noise, Δf is the offset frequency, fosc is the oscillation frequency and P is the power dissipation. The FOM of the PLL achieved 5-dB improvement comparing with the referred PLLs [3-5].

4. Conclusions

The 1/f-noise reduction technique of the SBC and the current source in the triode region is proposed. The SBC and the current source reduced the phase noise of the ring VCO by 3-dB and 7-dB, respectively. The ring VCO with 1-GHz oscillation achieved -68-dBc/Hz at 100-kHz offset, 710-μW power dissipation at 1-V power supply.

Acknowledgements

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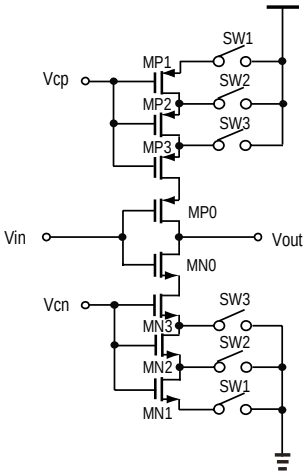

Fig. 1 Schematic of ring-VCO delay cell.

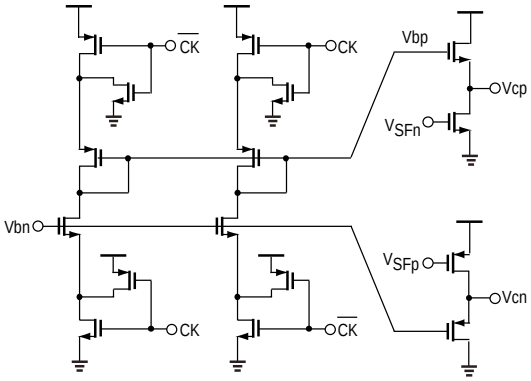

Fig. 2 Schematic of switched bias circuit.

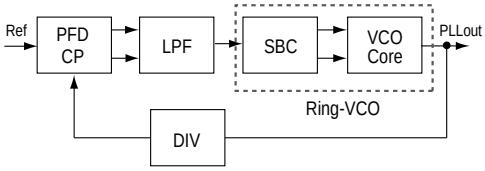

Fig. 3 Block diagram of PLL.

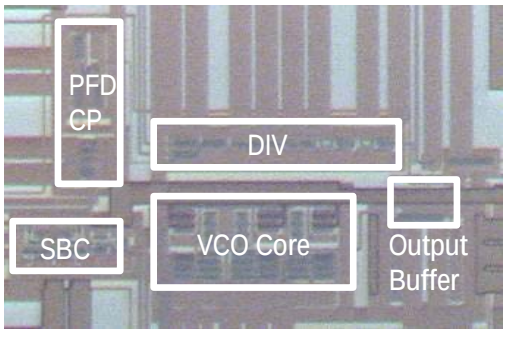

Fig. 4 Chip micrograph of PLL.

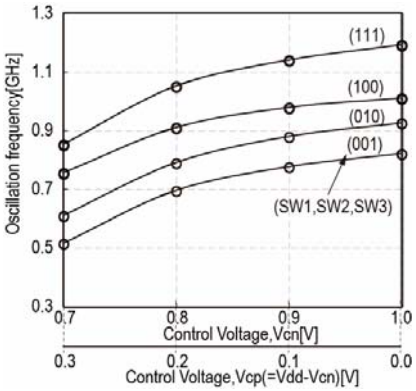

Fig. 5 Measured oscillation frequency by control voltage.

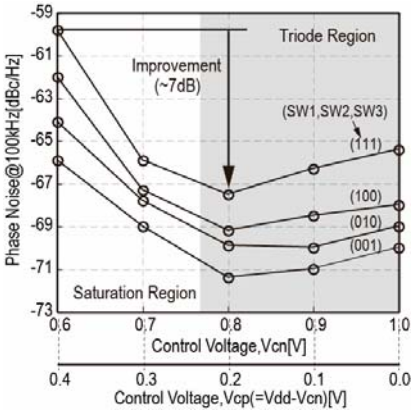

Fig. 6 Measured phase noise of the VCO at 100 kHz offset.

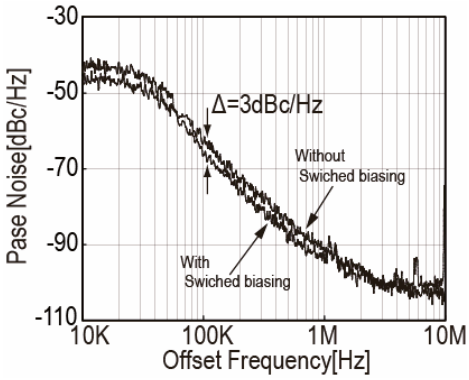

Fig. 7 Phase noise of PLL for a 1-GHz output with/without SBC.

Table 1 Performance Comparison

	Ref[3]	Ref[4]	Ref[5]	This Work
Supply voltage [V]	3.3	1.8	3.3	1.0
Process [μm]	0.35	0.18	0.35	0.18
Frequency range [GHz]	0.435-0.485	4.9-5.3	2.4-2.5	0.5-1.2
Phase noise [dBc/Hz]	-99 @100k	-121 @10M	-97 @1M	-92 @1M
Power [mW]	120	10	49.5	1.2
FOM [dBc/Hz]	-152	-166	-148	-171