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Fabrication of III-V-O-I (III-V on Insulator) structures on Si using micro-channel epitaxy with a two-step growth technique

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1. Introduction

Recently, III-V compound semiconductors are attracting considerable attention as channel materials for future advanced MISFETs with high performance, owning to their high electron mobility. Here, in order to utilize III-V materials on a Si platform, the formation of III-V compound semiconductors on Si substrates is mandatory. Furthermore, thinking of the application of them to short channel MISFETs, III-V-On-Insulator (III-V-O-I) structures are favorable because of the immunity for short-channel effects and the applicability to multi-gate structures. As one of ultimate CMOS structures, thus, we have proposed CMOS composed of III-V-O-I n-MISFETs and GOI (Ge-On-Insulator) p-MISFETs, shown in Fig. 1 [1]. One of the most critical issues on realizing this device is the fabrication of high quality and ultrathin III-V-O-I structures having high electron mobility. Therefore, crystal growth technologies, which form III-V materials with high crystallinity on insulators, are quite important. However, such a method has not been established yet.

One possible approach to grow III-V materials on insulators is the micro-channel epitaxy (MCE) [2], where the lattice information is transferred through narrow micro-channels, while the transfer of defect information is prevented by the presence of amorphous films covering substrates except for the micro-channel regions having the epitaxial layer-substrate interfaces. While this method is effective in reducing dislocations, another serious problem on III-V material growth on Si is the generation of anti-phase domains (APDs). In order to eliminate both dislocations and APDs, we propose a novel method, where a two-step growth technique including low temperature buffer layer growth is combined with MCE, for the first time. Fig. 2 schematically shows the proposed method. Here, while the APD generation can be suppressed by the two-step growth, the selective growth of the LT buffers is needed for the successful combination with MCE.

2. Experiments

As starting materials, we have used Si (110) substrates [3], because it is known to be difficult to eliminate APDs for the growth on (100) substrates even by the two-step method. GaAs epi-layers were grown by solid-source molecular beam epitaxy (MBE). The patterning of micro-channel was performed by photolithography on 100nm-120nm-thick thermal-oxide SiO_2 films.

GaAs layers were grown on the substrate using a two-step growth method. The procedure of the growth is shown in Fig. 3. First, a 10nm-thick GaAs buffer layer was grown at low temperatures at a rate of 0.5μm/h. Here, since the growth temperature of the LT buffer layers, T_{LT}, is a critical process parameter, T_{LT} was varied in a wide range of temperatures. This is because the selectivity of the buffer layer growth and APDs are strongly dependent on T_{LT}. Second, a 100nm-thick GaAs layer was grown at a fixed temperature of 600-630C at a rate of 0.5μ/h. The amount of APDs in the grown layer and selectivity was evaluated by the surface morphology observation.

3. Results and Discussions

It is found from the experiments with changing T_{LT} that the selective growth is obtained more easily with an increase in T_{LT}, while the amount of APDs is suppressed more with a decrease in T_{LT}. These facts mean that we need to find an appropriate temperature range of T_{LT}, where the two requirements on the selectivity and APDs are simultaneously satisfied.

The surface morphologies of the samples grown at typical T_{LT} are shown in Fig. 4. Also, the experimental results of the morphologies and the selectivity are summarized in Table. 1. It should be noted here that epi-layers with APDs do not have mirror-like surface morphology. It is found that, at T_{LT} lower than 410 C, the GaAs epi-layers have perfect mirror-like surface morphologies, while almost mirror-like and partly cloudy morphologies are obtained at T_{LT} between 460 C and 510 C. The APD generation can be effectively suppressed for the two-step growth at T_{LT} lower than 510 C. On the other hand, the selective growth is obtained at T_{LT} higher than 510 C. It is found, as a result, that 510 C is the appropriate growth temperature for the LT buffers from the viewpoints of the selective growth and the suppression of APDs.

In order to demonstrate the effectiveness of the proposed method, we fabricated III-V-O-I structures on a Si substrate, shown in Fig. 5. First, a 10nm-thick GaAs buffer layer was grown at T_{LT} of 510 C, which is the best temperature condition. Second, a GaAs layer of as thick as 4 μm was grown at 630 C so as to provide the lateral over-growth of GaAs on SiO_2. A TEM photo of fabricated samples (Fig. 6) clearly shows a III-V-O-I structure on a Si substrate. It is confirmed that there are no dislocations on SiO_2 owing to MCE. A clear lattice image of the GaAs layer on SiO_2, shown in Fig.6, strongly suggests the high crystallinity of GaAs-O-I fabricated by the proposed method.

4. Summary

We have proposed a novel method which can form III-V-O-I structures with less dislocations and APDs on Si substrates. We have successfully fabricated GaAs-O-I structures and verified the high crystallinity through the optimization of the growth temperature of the buffer layer.

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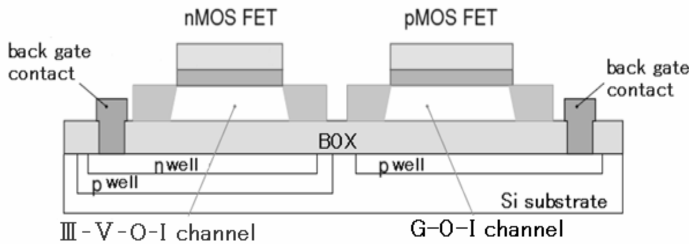


Fig.1 One example of ultimate CMOS structures [1]. III-V-O-I channels are used for high performance nMOSFETs.

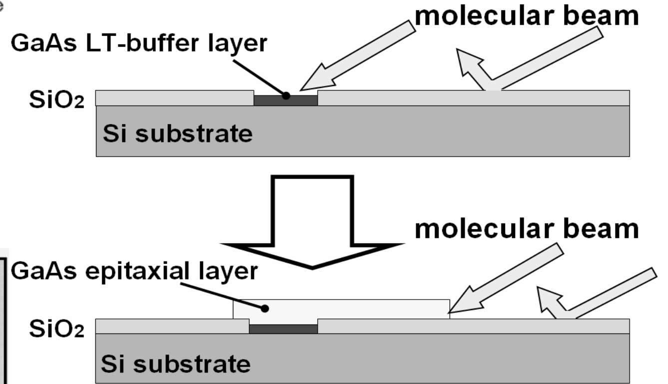


Fig.2 Proposed fabrication technique of III-V-O-I on a Si substrate. A LT-buffer layer can eliminate APDs, and MCE yields an epi-layer on SiO_2 with no dislocations.

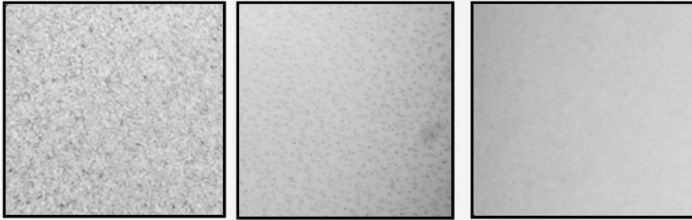


Fig. 4 (a) (b) (c)
An example of cloudy surface morphology : the lower growth temperature is 560C. An example of almost mirror-like surface morphology : the lower growth temperature is 460C An example of mirror-like surface morphology : the lower growth temperature is 360C.

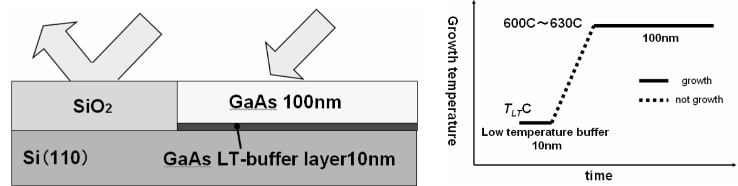


Fig.3 Procedure of the two-step growth in the proposed method

Table1 Summary of the experimental resutls of morphology and selectivity as a parameter of T_{TL}, which represents the growth temperature of the low temperature buffer.

T_{LT}[℃]	morphology	selective growth
580	cloudy	YES
560	cloudy	YES
510	almost mirror-like	YES
460	almost mirror-like	NO
410	perfect mirror-like	NO
360	perfect mirror-like	NO

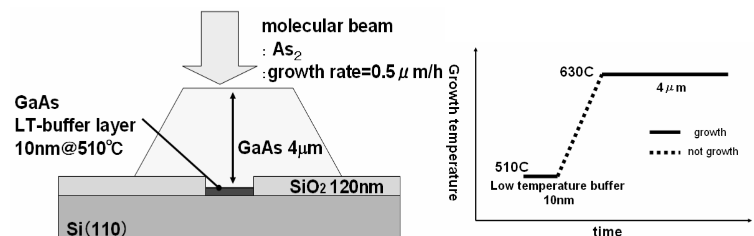
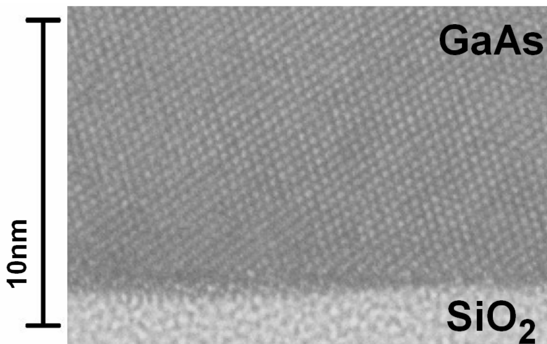


Fig.5 Sample structure for demonstrating III-V-O-I on a Si substrate using the combination of the two-step method and MCE.



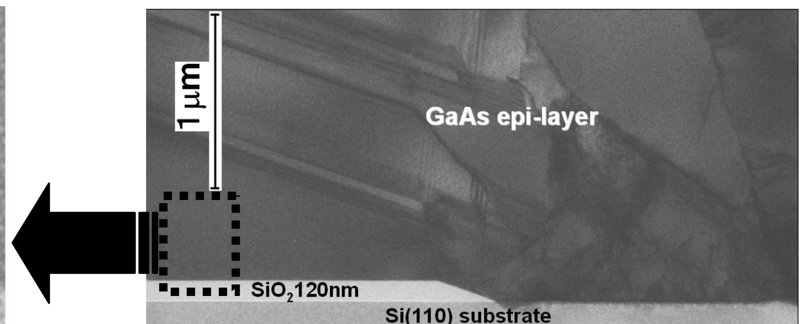


Fig. 6 Cross-sectional TEM microphotograph of GaAs on a Si substrate with SiO_2 mask . There are no dislocations in GaAs on SiO_2. The lattice image of GaAs on SiO_2 is clearly observed.

Fig. 5 Cross-sectional TEM microphotograph of GaAs grown on SiO_2 . The lattice image of GaAs is observed clearly.