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Towards metal gate/high-k dielectric integration for high performance CMOS technology

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1. Introduction

Dielectrics with high dielectric constant (high-k dielectric), such as Al_2O_3, ZrO_2, HfO_2, are widely studied as a replacement dielectric for SiO_2 in Si-based field effect transistors (FETs) with the initial intent to reduce the gate tunneling current which becomes unacceptably large with ultra-thin nitrided SiO_2 (SiO(N)) [1,2]. By now it has been widely demonstrated that dramatic gate leakage reductions can be achieved with high-k dielectrics. However, many of the other fundamental transistor parameters have been found to be adversely affected when compared to state-of-the-art FETs with SiO(N) dielectrics and polycrystalline Si (poly-Si) gate electrodes; 1) The channel electron mobility can be severely degraded by the presence of high-k dielectrics, 2) Threshold voltage control is found to be difficult, and 3) High defect densities in the bulk of the dielectric often result in poor threshold voltage, V_t, stability during FET operation [1,2].

After many years of research, the gate stack choices have been narrowed down to Hf-based dielectrics; predominantly HfO_2, HfSiO(N). In this abstract, some recent developments in the understanding and fabrication of HfO_2 FETs will be summarized.

2. Metal Gate Electrodes

Poly-Si gate electrodes are abandoned for scaling purposes. With metal gates, poly-Si depletion is eliminated, yielding an increased gate capacitance corresponding to about 0.4 nm in SiO_2 thinning, which is significant. In addition, difficulties with threshold voltage control for poly-Si electrodes on HfO_2 [3] have also initiated a wide search for suitable metal electrodes. Thirdly, it was reported that the formation of metal electrodes on HfO_2 can be less damaging to the dielectric as compared to the CVD poly-Si deposition process, providing enhanced stability during operation [4].

3. Control of Basic Transistor Properties

3.1 Channel Electron and Hole Mobility

In the early days of high-k research, transistors were plagued with notoriously low electron mobility [1,2]. Recently, high electron mobility values have been achieved in nFETs with HfO_2 gate dielectrics for several different metal gates [5-8], demonstrating that the performance of metal/HfO_2 stacks can be optimized in a conventional self-aligned process to match the performance of scaled poly-Si/SiON stacks without using intentional strain [7]. High thermal budgets are found to be beneficial for performance [7], which in turn can adversely impact the threshold voltage in self-aligned metal-gated transistors [9]. The performance of pFET is less of a concern, as the mobility is inherently lower on the Si (100) surface.

3.2. Threshold Voltage and Flatband Voltage Control

Threshold voltage control in poly-Si gated FETs with HfO_2 dielectrics remains extremely difficult, likely because Si reacts with Hf in the gate dielectric during deposition [10] and effectively pins the Fermi level at the dielectric/poly-Si interface [3]. This fact limits the application of poly-Si gates to low power applications, where relatively high threshold voltages (~ 0.5 V) are used [11]. To overcome this limitation, metal gate electrodes on HfO_2 have been intensely studied. Low workfunction metals like Ti, Ta, and V suffer from high reactivity. Metal nitride electrodes typically yield stable gate stacks, but the effective workfunctions is near midgap. Elemental high workfunction gate electrodes for pFETs like Pt, Re, or Ru exhibit extreme instabilities with respect to oxygen and hydrogen contaminations in the CMOS process [12-14]. The flatband voltage for MOS capacitors with Re electrodes was shown to vary by as much as 750 mV, depending on processing conditions [13]. Trace levels of O_2 in nitrogen can dramatically shift the flatband voltage at temperatures as low as 300 ^oC [13]. Similarly, post processing in a H_2 or H_2O containing inert ambient was shown to reduce the flatband voltage by more than 500 mV [13, 14]. These observations may be related to a modulation of the oxygen vacancy concentration in HfO_2 as discussed by Shiraishi, *et al*. [15]. Oxygen vacancies are thought to form easily in HfO_2 due to electron transfer from the neutral oxygen vacancy in HfO_2 to the metal, resulting in positively charged oxide defects. Recently, Pantisano, *et al*. [14] studied the impact of H_2 and O_2 anneals at temperatures below 600 ^oC using Ru electrodes on both SiO_2 and HfO_2 and confirmed the extraordinary sensitivity of the MOS capacitor flatband voltage to the presence of these chemical species for both dielectrics. Therefore, it was suggested that metal oxide and/or hydroxyl formation at the interface between the dielectric and the metal may lead to the formation of a dipole layer and either increase or decrease the effective workfunction of the gate stack.

To gain threshold voltage control, the use of capping layers on top of the HfO_2 and HfSiO dielectric has been intensely explored [8, 16].

In the case of pFETs, ultra-thin capping layers of Al_2O_3 and AlN have been demonstrated to lower the V_t by as much as 300 mV without substantial penalties in EOT, mobility and gate stack stability [16]. The physical/chemical origin of this shift remains unclear.

For nFETs, the fabrication of band-edge (BE) devices with an HfO_2 dielectric and a TiN/poly-Si gate electrodes has been demonstrated by using capping layers of La or Mg [8]. Band-edge devices were manufactured in a self-aligned process with 1000 ^oC, 5s gate activation, yielding excellent mobility at an inversion thickness of 1.4 nm. The capping layer was shown to intermix with the gate stack and it was therefore suggested that the V_t shift induced by capping layers containing group IIA and IIIB elements on HfO_2 may be due to the formation of positively charge oxygen vacancies (V_o^{++}). The vacancies form upon substitution of Hf^{4+} in HfO_2 with lower valence La^{3+}, for example [8].

It should be emphasized, that the detailed mechanism for the observed effective workfunction changes by capping layers are still under intense investigation and it can be expected that a better understanding will help in optimizing the gate stacks and hopefully contribute to the development of a stable pFET gate stacks with the desired BE effective workfunction.

3.3 Defects, Charge Trapping and Threshold Instability

In nFETs with HfO_2 dielectrics and poly-Si electrodes, the V_t stability during FET operation is reported to be systematically poor. The instability is attributed to HfO_2 defects, possibly oxygen vacancies in various charge states, which form during the poly-Si deposition [17, 18]. Theoretical calculations predict that the oxygen vacancy produces several defect levels in the HfO_2 bandgap which are in the immediate vicinity of the Si conduction band [19]. The existence of shallow defect levels was independently postulated based on the charging and discharging behavior of SiO_2/HfO_2 gate stacks under positive and negative bias stress [18]. Recently, an electrical technique was introduced to directly measure the energy distribution of electron traps, confirming the theoretically predicted energy level spectrum for oxygen vacancies defects [20].

Much improved stability is observed with some metal gates such that aggressively scaled nFETs exhibit acceptably low positive bias temperature instability [4].

4. Conclusions

Substantial improvements in the deposition methods for Hf based gate dielectrics – HfO_2 and HfSiO(N) – on silicon allow the deposition of very thin high-k dielectrics films on Si substrates, routinely yielding equivalent oxide thickness values of < 1 nm, as required in future CMOS technologies.

From a performance point of view, a mobility penalty has to be paid because of scattering with soft-optical phonon in the HfO_2 [21]. This scattering can be reduced by using SiO_2 buffer layers between the Si substrate and the HfO_2 dielectric [21]. These buffer layers also guarantee a high quality buried Si surfaces with low interface state density, and its presence reduces Coulomb scattering from remaining remote charged defects in the high-k layer. All these facts allow the fabrication of aggressively scaled gate stacks which exhibit mobility values which are competitive with those measured in nFETs with SiON dielectrics.

Threshold voltage control for the pFET devices remains challenging. More work is needed to understand the strong processing dependence of the threshold voltage, but it has now become clear that the defect properties of the high-k layer itself and the interaction between the dielectric and the electrode are a major factor in establishing the threshold voltage. The presence or absence of small amounts of oxygen and/or hydrogen during gate stack fabrication, the temperature and thermal budget all can dramatically change the threshold voltage of pFETs. Various methods have been developed to gain threshold voltage control. The concept of ultra-thin dielectric cap layers onto the high-k film has been successfully used to shift effective workfunctions towards lower values for both n and pFETs.

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