Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Yokohama, 2006, pp. 208-209

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Demonstration of Low V_t NMOSFETs Using Thin HfLaO in ALD TiN/HfSiO Gate Stack

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Abstract: The effect of a HfLaO capping layer in an atomic layer deposition (ALD) HfSiO/TiN gate stack is investigated. It is found that La diffusion and accumulation near the interface with the Si substrate, strongly enhanced by annealing process, could be the primary cause of threshold voltage (V_t) shift and mobility degradation.

Introduction

High-k gate dielectrics and metal electrodes are currently being investigated for the highly scaled MOSFET devices. For NMOSFETs, the work function is required to be within 0.2 eV of the Si conduction band, which can lead to a threshold voltage (V_t) value of about 0.3 V, without channel engineering. Identifying metal electrode materials with such work function values on high-k dielectrics is challenging due to the effects of Fermi level pinning, fixed charges, and thermal instability of the gate/dielectric interface. Alternative approaches to achieving the proper V_t values involve the dielectric capping layer [1,2], as well as an additional metal layer inserted at the electrode/dielectric interface [3,4]. In this study, we investigate the effect of introducing a HfLaO capping layer HfO_2 gate dielectric on the performance of high-k NMOSFETs with the TiN gate electrode.

Experiment

NMOSFETs were fabricated using a conventional CMOS process flow with a 1070ºC spike anneal after source/drain implantation, followed by a forming gas anneal (FGA). A pre-gate clean was performed using dilute HF or O_3/deionized (DI) water before the deposition of 2.0 nm HfSiO film. Following the HfSiO deposition, HfLa (50% Hf/50% La) was sputtered on and a rapid thermal anneal (RTA) was conducted at 600ºC under atmospheric pressure, forming about 1.0 nm of HfLaO. A post-deposition anneal (PDA) at 700ºC in NH_3 ambient was performed either before or after HfLaO formation (Table 1 & 2). The gate electrode was 10 nm of ALD TiN film followed by 100 nm amorphous silicon.

Results and Discussion

A process flow for fabricating NMOSFETs with an ALD TiN/HfSiO gate stack and HfLaO capping layer is described in Table 1. Fig.1 shows the flat-band voltage (V_{fb})-equivalent oxide thickness (EOT) plot, which was used to extract the effective work function of metal gates in the HfLaO/HfSiO stacks. The effective work function of ALD TiN gate with HfLaO was estimated to be as low as 4.2 eV, which is about 300 mV lower than that of TiN without HfLaO. Reductions in effective work function by HfLaO were consistent with the results of the La_2O_3/HfSiO gate stack [5], which could be explained by bulk charges, dipole formation, band-offset changes, or Fermi level pinning due to La incorporation into HfSiO by a reaction of HfSiO and HfLaO. The capacitance-voltage (C-V) and drain current (I_d)-gate voltage (V_g) curves also show V_{fb} and V_t shift caused by HfLaO, which are consistent with the work function difference (Fig. 2 & 3). However, effective mobility degrades in the NMOSFETs with a HfLaO cap (Fig. 4). This mobility degradation could be due to the interface states (N_{it}) increase by La diffusion to the interface with Si substrate (Fig. 5).

To further investigate the effect of La diffusion by the subsequent annealing processes, a TiN-gated NMOSFET with a HfLaO/HfSiO gate stack was fabricated without the 700ºC PDA (Table 2). Fig. 6 shows Si 2*p* and La 4*d* XPS spectra of oxidized and annealed HfLa on HfSiO. Clear La-O bonding is observed after both the 600ºC RTA only and the 600ºC RTA followed by 700ºC annealing. Fig. 7 shows a high resolution transmission electron microscopy (HRTEM) cross-section image of the NMOSFET with a HfLaO/HfSiO gate stack. The HfLaO layer is not clearly distinguished suggesting HfLaSiO formation by the reaction of HfSiO and HfLaO. Although a 700ºC PDA is skipped, HfLaO-induced V_{fb} and V_t shifts are observed (Fig. 8, 9, & 10). It is seen that the amount of V_{fb} (V_t) shift is less in the NMOSFET fabricated with the 700ºC PDA. The effective work function estimated from the V_{fb} (V_t) difference is about 4.3 eV, which is about 100 mV higher than that of TiN on HfLaO/HfSiO fabricated without the 700ºC PDA. The work function can be further reduced by replacing TiN with thin ALD TiN (fig. 1) or ALD HfSiN [6], which has a lower work function than 10 nm of TiN. The effective mobility of HfLaO/HfSiO without the 700ºC PDA is comparable to that of the control HfSiO (Fig. 11), thus the N_{it} are expected to be comparable to the control HfSiO. Fig. 12 shows N_{it} measured by the charge pumping method. The difference is not significant, suggesting less La diffusion due to the low thermal budget right after HfLaO formation.

To verify La concentration near the Si substrate interface, secondary ion mass spectroscopy (SIMS) profiles were obtained on devices with HfLa on HfSiO annealed at 600ºC only and at 600ºC followed by a 700ºC anneal (Fig. 13). The trend in mobility degradation is consistent with the La counts in the dielectric near the interface with Si substrate, suggesting that La near the interface is enhanced by subsequent thermal processing, which affects interface states and, subsequently, the channel carrier transport.

Conclusion

In conclusion, it was determined that the HfLaO capping layer tends to intermix with the HfSiO, thereby lowering the effective work function and V_t. However, La diffuses towards the interface with the Si substrate, increasing the interface states, which could be the primary cause of mobility degradation. Therefore, to improve device performance, an optimized process sequence using a reduced thermal budget would be required to control La diffusion.

References

[1] H.-J. Li,et al., *IEEE EDL*, vol. 26, no. 7, pp. 441-444, 2005.
[2] H.-S. Jung, et al., *VLSI Tech.*, 2005, pp. 12B-4.
[3] Y. Shimamoto et al., *VLSI Tech.*, 2005, pp. 8A-4.
[4] R. I. Hegde et al., *IEDM Tech*. Dig., 2005, pp. 2.4.
[5] H.N. Alshareef et al., *VLSI Tech*., 2005, pp. 2.1.
[6] K. Choi et al, to be presented at ALD conference 2006.

- Pre-gate clean
- HfSiO 2.0 nm
- HfLa sputtering
- ***RTA at 600℃ in N_2***
- ***PDA at 700℃ in NH_3***
- ALD TiN 10.0 nm
- polysilicon 100.0 nm
- spike annealing at 1075C
- gate etch

Table 1. Process flow of NMOSFET with HfSiO/ HfLaO gate stack formed by 600°C followed by 700°C PDA step.

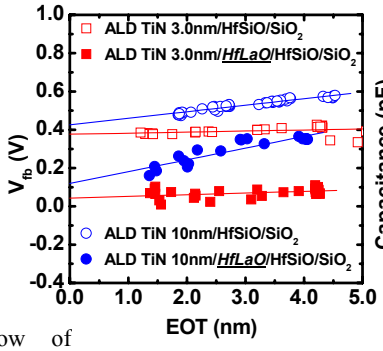

Fig. 1 Plots of V_{fb} vs. EOT for $HfSiO/SiO_2$ and HfLaO/HfSiO/ SiO_2.

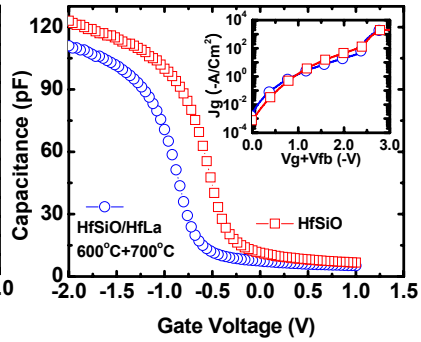

Fig. 2 C-V curves (at 1 MHz) of $TiN/HfSiO/SiO_2$ and HfLaO/ $HfSiO/SiO_2$

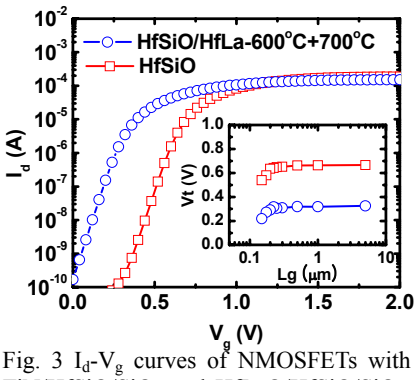

Fig. 3 I_d-V_g curves of NMOSFETs with $TiN/HfSiO/SiO_2$ and $HfLaO/HfSiO/SiO_2$. Inset figure shows V_t vs. gate length of both gate stacks.

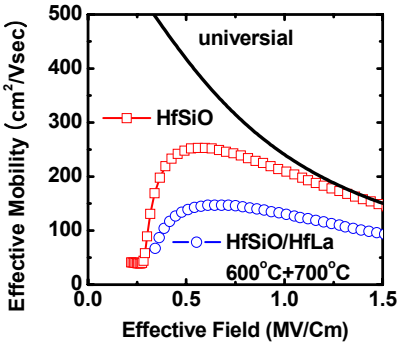

Fig. 4 Effective carrier mobility of NMOSFETs with $TiN/HfSiO/SiO_2$ and $HfLaO/HfSiO/SiO_2$.

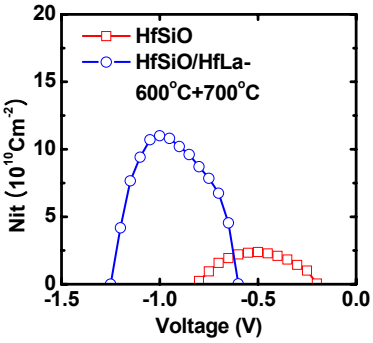

Fig. 5 Nit of NMOSFETs with $TiN/HfSiO/SiO_2$ and $HfLaO/HfSiO$ $/SiO_2$.

- Pre-gate clean
- HfSiO 2.0 nm
- HfLa sputtering
- RTA at 600°C in N_2
- ***skip anneal at 700℃***
- ALD TiN 10.0 nm
- polysilicon 100.0 nm
- spike annealing at 1075C
- gate etch

Table 2. Process flow of NMOSFET with HfSiO/ HfLaO gate stack formed by 600°C only.

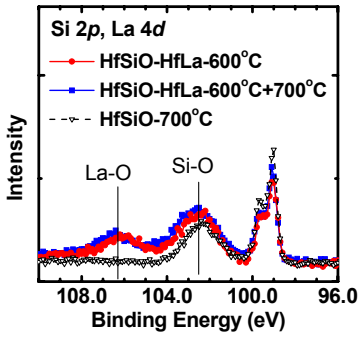

Fig. 6. Si 2p and La 4d XPS spectra of HfSiO and HfLaO/HfSiO dielectrics. La-O bonding is observed both annealed samples .

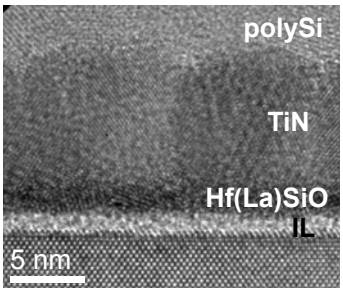

Fig. 7. HRTEM image of cross section of polySi/TiN/HfLaO /HfSiO gate stack.

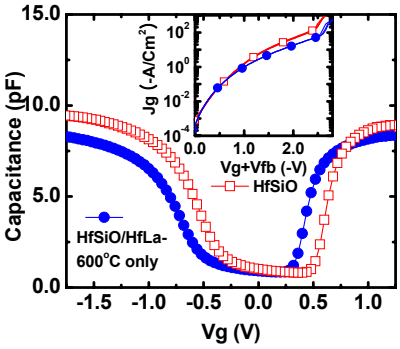

Fig. 8 High frequency C-V curves of TiN gated NMOSFETs with HfLaO/HfSiO and HfSiO gate stacks. The inset figure shows gate leakage currents of MOS capacitors with both gate stacks measured under accumulation condition.

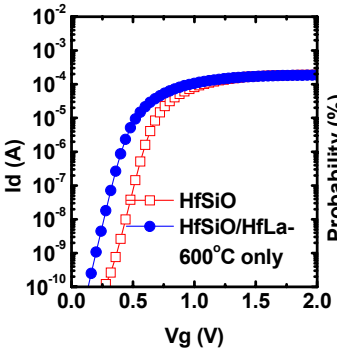

Fig. 9. I_d-V_g curves of NMOSFETs with TiN/ $HfSiO/SiO_2$ and HfLaO/ $HfSiO/SiO_2$.

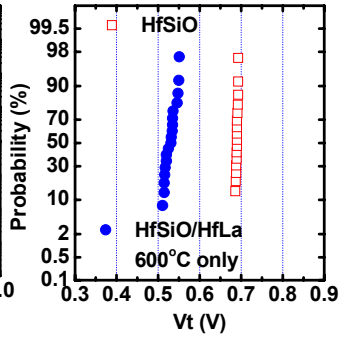

Fig. 10. Cumulative V_t of long channel NMOSFET (W/L=10/5.0).

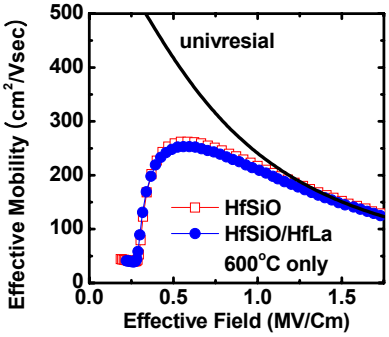

Fig. 11. Effective carrier mobility of NMOSFETs with $TiN/HfSiO/SiO_2$ and $HfLaO/HfSiO/SiO_2$ with 600°C PDA only.

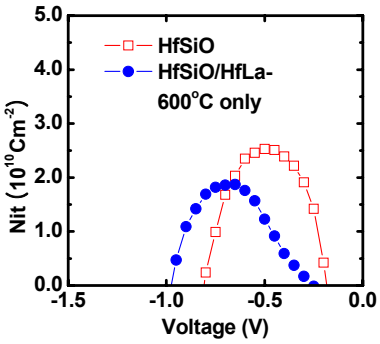

Fig. 12. N_{it} of NMOSFETs with $TiN/HfSiO/SiO_2$ and $HfLaO/HfSiO$ $/SiO_2$.

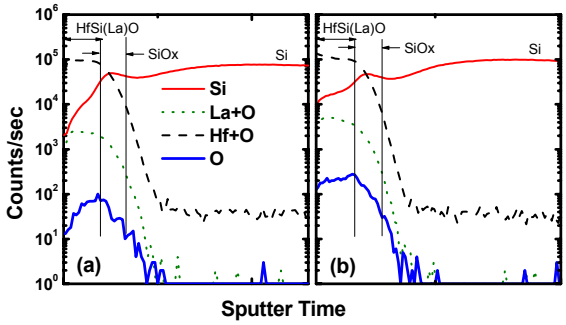

Fig. 13. SIMS analysis of HfSiO/HfLa followed by (a) 600°C PDA only and (b) 600°C + 700°C PDA. Analysis were made after polySi and TiN were removed.