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High quality La aluminates/Si (100) interface realized by passivation of Si dangling bonds with one monolayer epitaxial $SrSi_2$

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1. Introduction

La aluminates (LAO) with large conduction band offset against Si (ΔE_c=2.4 eV) are eminently suitable for high-k gate dielectrics in 22 nm CMOS technology. Recently, low leakage current with thin equivalent oxide thickness (T_{ox}=0.3 nm) has been realized by using LAO [1]. However, interface trap density (D_{it}=5x10^{12} $cm^{-2}eV^{-1}$) was relatively high, similar to other high-k oxides [2]. Some attempts to passivate Si dangling bonds (DB) by alkaline earth metals were pursued for suppression of interface traps [3-8]. In particular, it was predicted that Sr atoms could passivate Si DB without interface trap states in the bandgap of Si [5]. Until now, crystalline Sr titanates (STO) films were experimentally formed on a Sr-terminated Si surface [6-8]. However, STO films are difficult to apply for CMOSFET because of small ΔE_c [7].

In this study, amorphous LAO films were deposited on the Si surface passivated with 1 monolayer (ML) epitaxial $SrSi_2$. We demonstrated that 1 ML epitaxial $SrSi_2$, which passivated Si dangling bonds, considerably suppressed interface traps between amorphous LAO and Si.

2. Experiment

1 ML epitaxial $SrSi_2$ and LAO films were formed on n-type Si substrates by molecular beam epitaxial techniques. LAO films were deposited by using Al and La metal sources at 600 °C in O_2 ambient with a flow rate of 0.1 sccm. MOS capacitors in which Mo was used as a gate electrode were fabricated for CV and IV measurements.

3. Results and Discussion

3.1. Formation process of 1ML epitaxial $SrSi_2$

Fig. 1 shows the formation process of 1 ML epitaxial $SrSi_2$. Surface structures were monitored by in situ RHEED. After HF-treated Si was transported to UHV (<10^{-10} torr) chamber, a H-terminated Si (100) 1x1 surface was observed (Fig. 2(a)). During annealing up to 500 °C, a clean Si (100) 2x1 surface was formed (Fig. 2(b)). Subsequently, an amount of Sr atoms corresponding to 2 ML $SrSi_2$ was deposited and then the pattern of the Si (100) 2x1 surface was blurred (Fig. 2(c)), which indicates the surface was covered sufficiently with Sr atoms. During annealing up to 800 °C, a sharp streak pattern indicating a well-ordered surface was observed (Fig 2(d)). This pattern is almost the same as that of the Si (100) 2x1 surface. However, it was confirmed that an amount of Sr atoms corresponding to 1 ML $SrSi_2$ remained on the surface by ICP-AES analysis. We believe that Extra Sr atoms desorbed from Si surface during annealing up to 800 °C. Therefore, these results of the well-ordered surface and the remaining amount of Sr indicate that 1 ML epitaxial $SrSi_2$ was prepared by control of our sophisticated epitaxial techniques. 1ML epitaxial $SrSi_2$ is probably the same atomic arrangement as the theoretically predicted surface in the lowest energy (Fig. 3)[5].

3.2. Electrical properties of LAO with or without $SrSi_2$

Fig. 4 shows cross-sectional TEM micrographs of LAO film deposited on 1ML $SrSi_2$ (LAO/Sr/Si) and on a bare Si (LAO/Si), respectively. Both micrographs show almost same physical thickness and no interfacial layer. The same T_{ox} (2.0 nm) and dielectric constant (ε=23) were obtained by CV measurements at 1 MHz (Fig. 5). 1 ML epitaxial $SrSi_2$ had no influence on T_{ox}. Fitting results of calculated CV curves, based on experimental characterization of SiO_2 MOS capacitor [9], were also shown in Fig. 4. D_{it} of LAO/Sr/Si and LAO/Si were estimated from flat band differences (ΔV_{fb}) between calculated curves and experiment CV data. D_{it} is given by

$$D_{it}=(\varepsilon_{ox}\cdot\Delta V_{fb})/(qT_{ox})\ [cm^{-2}eV^{-1}] \quad –(1)$$

where ε_{ox} and q are dielectric constant of SiO_2 and elementary charge, respectively. D_{it} of LAO/Sr/Si (6x10^{11} $cm^{-2}eV^{-1}$) was much smaller than that of LAO/Si (1.4x10^{12} $cm^{-2}eV^{-1}$). In addition, flat band voltage (V_{fb}) of LAO/Sr/Si almost corresponded to the ideal V_{fb} of 0.4V estimated by the difference of work function between Mo (4.6eV) and n-type Si (4.2eV). On the other hand, V_{fb} of LAO/Si was shifted negatively (–0.6 V), indicating that a large amount of positive fixed charge (Q_f) exists at the interface. Fig. 6 shows leakage current density (J_g) at $|V_g-V_{fb}|$=1V vs. T_{ox} for LAO/Sr/Si and LAO/Si with reported data of SiO_2, Hf-based oxide and LAO [1, 10-12]. J_g of our data were lower than those of other reported data. 1ML epitaxial $SrSi_2$ had negligible influence on J_g.

In summary, it was demonstrated that passivation of Si DB by 1 ML epitaxial $SrSi_2$, followed by LAO deposition, bring about suppression of D_{it} and Q_f with no degradation in EOT and J_g.

4. Conclusion

We developed the sophisticated passivation techniques for LAO/ Si (100) interface with 1 ML epitaxial $SrSi_2$. High quality LAO/Si (100) interface with low D_{it} and Q_f was realized by passivation of Si DB with 1 ML epitaxial $SrSi_2$, which is promising for improvements of CMOSFET performances with high-k gate dielectrics.

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References

[1] M. Suzuki et al., IEDM Tech. Dig., (2005)
[2] G. Lucovsky et al., Appl Phys. Lett., **74**, 2005(1999)
[3] T. Schimizu et al., Japanese patent, P2005-294564
[4] D.P. Norton et al., J. Vac. Sci. Technol., **B20**, 257(2002)
[5] C. J. Först et al., Nature, **427,** 53(2004)
[6] R.A. Mckee et al., Phys. Rev. Lett., **81**, 3014(1998)
[7] S. J. Walker et al., IEDM Tech. Dig., 955(2001)
[8] R. Droopad et al. J. Crystal Growth, **251**, 638(2003)
[9] N. Yasuda et al., Ext. Abstr. IWGI, 212(2001)
[10] M. I. Gardner et al., Ext. Abstr. IWGI., 31(2003)
[11] M. Koike et al., IEDM Tech. Dig., 107(2003)
[12] M. Hirose et al, Semicond. Sci. Technol., **15**, 485(2000)

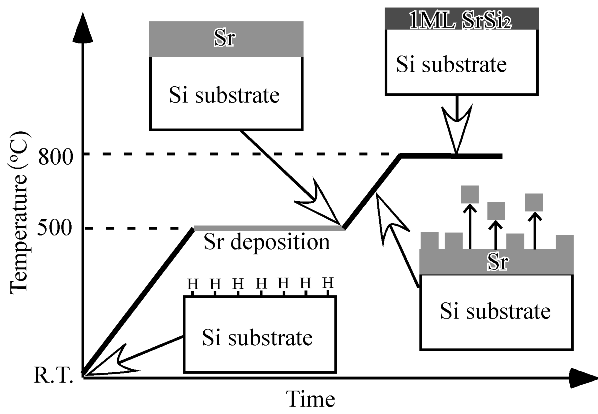

Fig.1. The details of 1ML epitaxial $SrSi_2$ formation process.

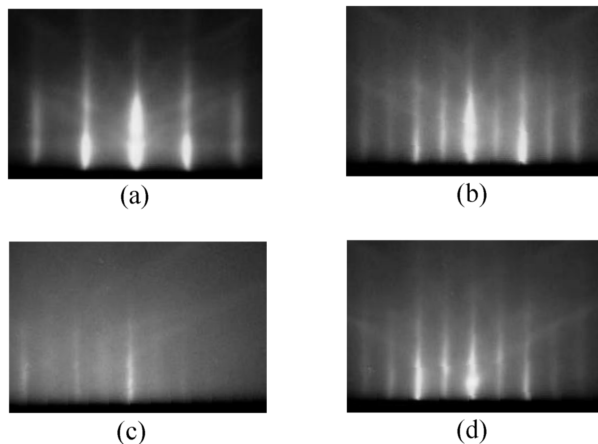

Fig.2. RHEED patterns along the Si<110> azimuth.

(a) a H-terminated Si (100) 1x1 surface
(b) a clean Si (100) 2x1 surface
(c) the clean Si (100) surface with 2ML Sr deposition
(d) the 2x1 surface of 1ML epitaxial $SrSi_2$

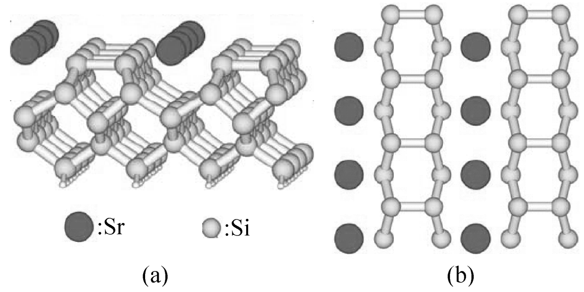

Fig.3 Schematic view of theoretically predicted 1ML $SrSi_2$ surface with the lowest energy ((a) side view and (b) plan view) [5].

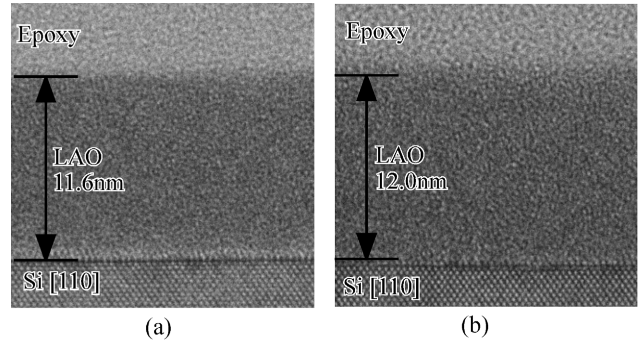

Fig.4. Cross-sectional TEM micrographs of (a)LAO/Sr/Si and (b) LAO/Si.

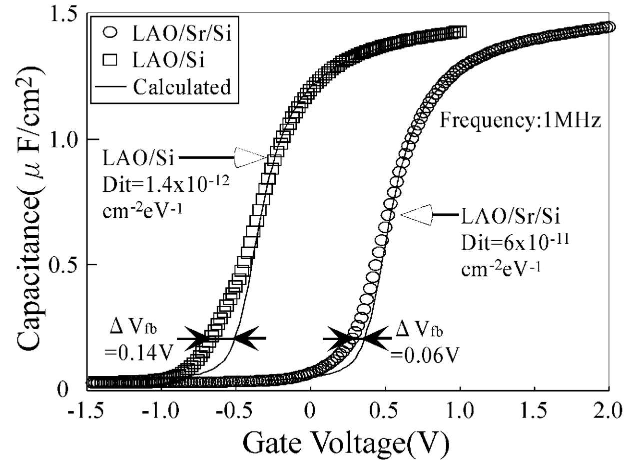

Fig.5.CV data of LAO/Sr/Si and LAO/Si with calculated CV curves based on experimental characterization of SiO_2 MOS capacitor [7].

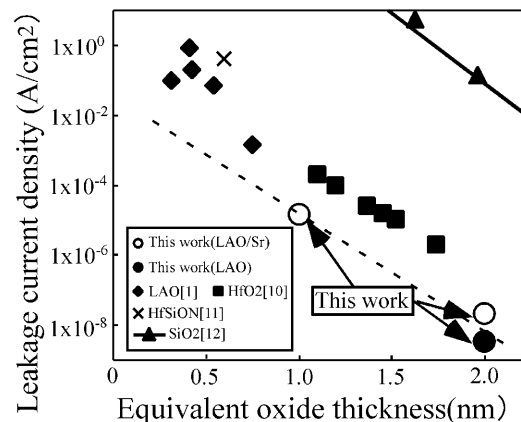

Fig.6 Jg at $|V_g-V_{fb}|=1V$ vs T_{ox} for LAO/Sr/Si and LAO/Si with reported data of SiO_2, Hf-based oxides and LAO [1,10-12].