Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Yokohama, 2006, pp. 1128-1129

J-10-1 Work Function Modulation by Segregation of Indium through Tungsten Gate For Dual-Metal Gate CMOS Applications

Kazuaki NAKAJIMA[1], Masato KOYAMA[2], Tomonori AOYAMA[1], Akira NISHIYAMA[2], Kazuhiro EGUCHI[1] and Kyoichi SUGURO[1]

[1]Semiconductor Company, Toshiba Corporation, 8 Shinsugita-cho, Isogo-ku, Yokohama 235-8522, Japan

[2]Research and Development Center, Toshiba Corporation, 8 Shinsugita-cho, Isogo-ku, Yokohama 235-8522, Japan

Phone/Fax: +81-45-770-3661/3577, e-mail: kazuaki2.nakajima@toshiba.co.jp

Abstract

We first propose work function modulation by using segregation of indium through W gate electrode. We studied electrical properties of MOS capacitor using W/In/W stacked gate. Compared to the W gate, flatband voltage (Vfb) of W/In/W stacked gate shifts toward negative gate bias of ~750mV after annealing at 600°C. The change of work function in W/In/W stacked gate structure is found to be due to Indium segregation to the interface between W and gate insulator through W grain boundary. We successfully demonstrate work function modulation of W gate from 4.8eV to 4.1eV by using indium segregation technique.

Introduction

Dual metal gate technology using two kinds of metal for nMOS and pMOSFETs is required to realize high performance CMOSFETs for hp 45nm generation and beyond [1]. However, the integration of dual metal gate formation is so complicated. Two kinds of damage-free metal deposition processing for nMOS and pMOSFETs are needed. Furthermore, metal removal processing of either metal gate is needed without degradation of reliability of gate insulator. On the other hand, work function is controlled by impurity segregation in fully silicided (FUSI) gate processing [2]. FUSI gate is compatible to conventional Si processing. However, it is reported that work function of Si-contained metal gate can not be controlled on High-k dielectric by pinning effect [3]. Therefore, metal gate material, which not consists of silicon, should be selected to realize dual metal gate on both SiO_2 and High-k gate insulator. In this report, we demonstrate a new method of work function modulation using segregation of indium through W film.

Experimental

We fabricated an MOS capacitor to examine work function of metal gate. Figure 1 shows process flow of MOS capacitor using W/In/W stacked gate. Thermal oxide was grown in the range of thickness from 5nm to 10nm. Metal gate is formed on the thermal oxide by DC-sputtering using metal mask. In this study, we prepared two kinds of gate structure, namely, 40nm-thick W gate and a stacked gate composed of 40nm-thick 2nd. W layer, 20nm-thick In layer, and 20nm-thick 1st. W layer. After gate formation, forming gas annealing was carried out at temperature in the range from 300°C to 600°C for 1 hour. We estimated work function from C-V measurement and barrier height from I-V measurement.

Results and discussion

Figure 2 shows C-V characteristics of MOS capacitors for both W gate and W/In/W stacked gate after forming gas annealing at 400°C. Compared to the W gate, Vfb of W/In/W stacked gate shifts toward negative gate bias of ~440mV. In order to examine work function in each case, we studied effective oxide thickness (Teff) dependence of Vfb. Work function is determined for W gate (5.0eV) and W/In/W stacked gate (4.6eV) as shown in Fig.3. We examined I-V characteristics of W gate and W/In/W stacked gate. No degradation of leakage current is found in either case (Fig.4). To estimate charge trapping for W/In/W stacked gate, we measured long-term variation of Vg at 0.1mA/cm^2 of constant current stressing. W/In/W stacked gate shows negligible charge trapping (Fig.5). These results suggest that gate oxide reliability does not degrade for W/In/W stacked gate. Figure 6 shows annealing temperature dependence on C-V characteristics. Even though Vfb on W gate does not change after 600°C annealing, Vfb on W/In/W is found to shift toward negative gate voltage with the increase of annealing temperature. After annealing at 600°C, W/In/W gate demonstrates negative Vfb shifts of ~540mV, compared to W gate. In order to confirm the accuracy of work function obtained from C-V measurement, we estimated barrier height from Fowler -Nordheim (FN) conduction by I-V measurement. Barrier height (Φ_{bh}) for W/In/W stacked gate is found to change from 3.9eV to 3.5eV with increment of annealing temperature (Fig.7). It is consistent with work function estimated from Vfb. In order to examine crystal orientation of W/In/W stacked gate, the X-ray diffraction (XRD) method was carried out. As shown in Fig.8, only W(110) peak is observed for W/In/W stacked gate. No signature, which means a formation of W-In metal alloy phase, is observed after N_2 annealing at 600°C. This result suggests that the ΔVfb does not relate to reaction of W with In. In order to verify a root cause of ΔVfb for W/In/W stacked gate, TEM observation was carried out (Fig. 9). The degradation of W/SiO_2 interface is not observed even if annealing temperature increases up to 600°C. We estimated content of indium in the W film and W/SiO_2 interface. As a result, no indium is observed in W grain. However, it is detected in W grain boundary and W/SiO_2 interface (Fig.10). Furthermore, it is noted that more indium is detected at the W/SiO_2 interface near W grain boundary. A model for segregation of indium through W films is shown in Fig.11. EDX- results suggest that indium easily diffuses through W grain boundary and segregates at the W/SiO_2 interface. We examined annealing temperature dependence on content of indium at the W/SiO_2 interface near W grain boundary. Indium segregated at the W/SiO_2 interface increases with increment of annealing temperature (Fig.12). It is well known that work function of indium is 4.12eV [4]. Therefore, these results suggest that work function of W/In/W stacked gate is determined by content of indium segregated at the W/SiO_2 interface. In order to accelerate diffusion of indium through W grain boundary, we examined annealing ambient dependence on Vfb for W/In/W stacked gate (Fig.13). Using forming gas annealing, it is found that Vfb of W/In/W stacked gate drastically shifts toward negative gate voltage of ~750mV. Indium is easily oxidized by exposure to air. Therefore, it is considered that much indium can be mobile by deoxidization of indium-oxide in forming gas annealing. Work function and barrier height for W gate and W/In/W stacked gate are summarized in Table 1. By combination with tungsten gate and segregation of indium, dual metal gate having work function of 4.1eV and 4.8eV is successfully realized.

Conclusion

We studied work function modulation by using segregation of indium through W gate electrode. For W/In/W stacked gate structure, it is found that indium diffuses through W film to the interface between W electrode and gate insulator with increase of annealing temperature. We have successfully demonstrated work function modulation of W gate from 4.8eV to 4.1eV by using indium segregation. In this method, work function of metal gate is controlled without two kind of metal deposition processing.

References

[1] S.B.Samavedam, et al., IEDM Tech. Dig. , 2002, pp.433
[2] J. Kedzierski, et al., IEDM Tech. Dig., 2003, pp.315
[3] E. Cartier, et al., VLSI Tech. Dig., 2004, pp.44
[4] H. B. Michaelson, J. Appl. Phys., Vol.48, pp.4729 (1977)

- **Gate oxidation (5nm, 8nm, 10nm)**
- **Gate formation by DC sputtering**
  Case1 : W(40nm)
  Case2 : W(10nm)/In(20nm)/W(40nm)
- **Annealing at 300°C -600°C for 1 hour in N_2 or forming gas ambient**

Fig.1 MOS capacitor process

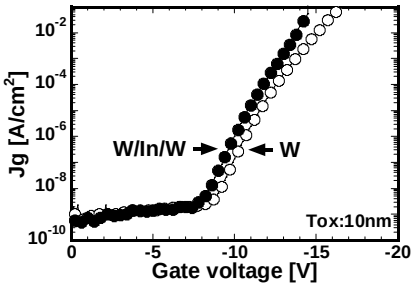


Fig.4 I-V plots of MOS capacitors for W gate and W/In/W stacked gate. Gate leakage current is not degraded for W/In/W stacked gate.

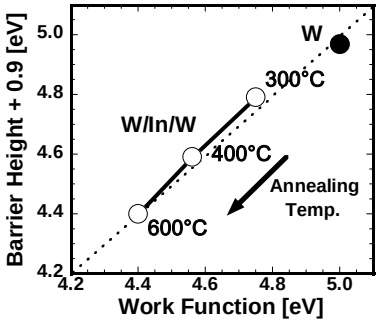


Fig. 7 Relationship between work function and barrier height for W gate and W/In/W stacked gate. Barrier height is consistent with work function. Barrier height decreases with increment of annealing temperature.

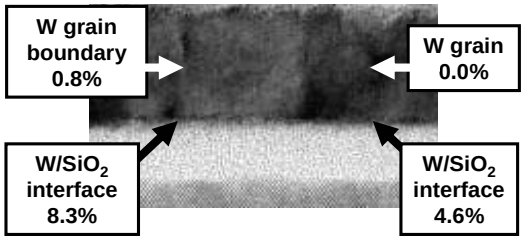


Fig.10 TEM image at the W/SiO_2 interface and Content of indium estimated by EDX analysis after annealing at 600°C. Though indium does not include in W film, indium is detected in W grain boundary and at W/SiO_2 interface.

Fig.13 (right) C-V curve of MOS capacitors for W gate and W/In/W stacked gate. After forming gas annealing at 600°C, drastically shift (~750mV) in Vfb for the W/In/W stacked gate is observed. It is considered that much indium can be mobile by deoxidization of indium-oxide, which forms in the air, in forming gas annealing.

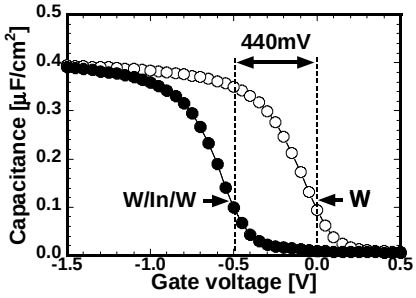


Fig.2 C-V curves of MOS capacitors (Tox:8nm) for W gate and W/In/W stacked gate. Vfb for the W/In/W stacked gate shifts toward negative gate voltage of ~440mV, compared to the W gate.

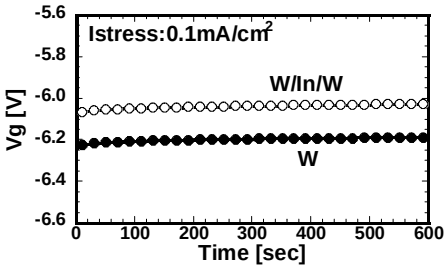


Fig.5 ΔVg-t plots for W gate and W/In/W stacked gate (Tox:5nm). W/In/W stacked gate shows negligible charge trapping.

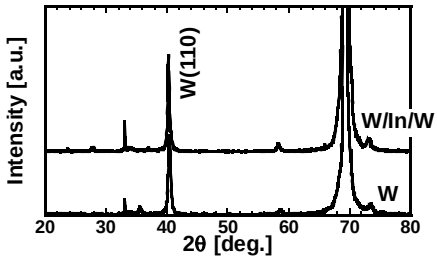


Fig.8 XRD Spectrum of W/In/W stacked film and W film after annealing at 600°C. No signature of formation of W-In alloy is observed.

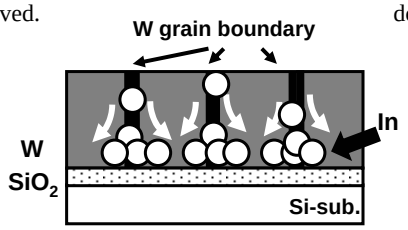
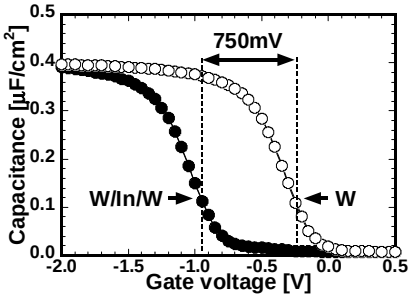


Fig.11 Model for segregation of indium through W films. Indium easily diffuses to W/SiO_2 interface through W grain boundary. More indium is detected at W/SiO_2 interface near W grain boundary.



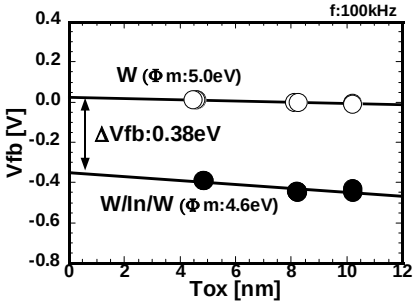


Fig.3 Teff dependence on Vfb for W gate and W/In/W stacked gate. Work function was determined for W (5.0eV) and W/In/W stacked gate (4.6eV).

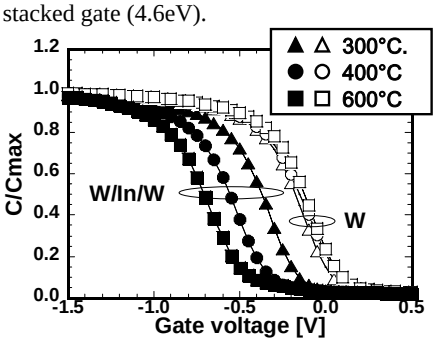


Fig.6 C-V curve of MOS capacitors for W gate and W/In/W stacked gate. Significant shift in Vfb for the W/In/W stacked gate is observed as annealing temperature increases.

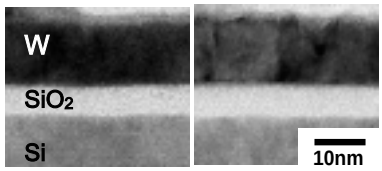


Fig.9 TEM images at the interface between 1st. W layer and SiO_2 for W/In/W stacked gate. (left) as-depo., (right) after annealing at 600°C. The W/SiO_2 interface does not degrade after annealing at 600°C.

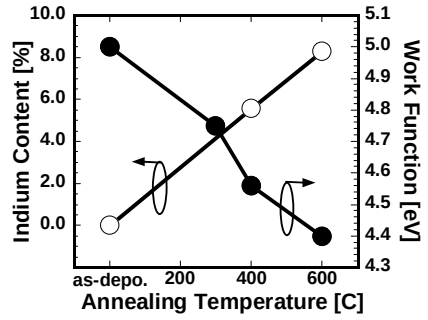


Fig.12 Content of indium is estimated by EDX analysis. Indium at the W/SiO_2 interface increases with increment of annealing temperature. Work function of W gate is controlled by segregation of indium.

Φm [V]		ΔΦm [V]	Φbh [eV]		ΔΦbh [eV]
W	W/In/W		W	W/In/W	
4.80	4.06	0.74	3.94	3.24	0.70

Table 1 Work function and barrier height of W and W/In/W stacked gate on SiO_2 .