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Diffusion control technique in TiN stacked metal gate electrodes for p-MISFETs

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1. Introduction

For conventional CMIS devices, p+ or n+ poly-Si are used as a gate electrode. However, the depletion of the poly-Si gate electrode becomes problem in the continuous scaling. Moreover, the application of high-k gate dielectrics with the combination of poly-Si gate electrodes causes the shift of the threshold voltage to be higher by Fermi-level pinning, especially in p-MISFETs [1, 2]. To avoid these problems, metal gate electrodes are required for next generation devices [3]. For the materials of metal gate electrodes, the properties are needed as follows, A): suitable work function values for p- (4.8-5.1eV) and n-MISFETs (4.0-4.3eV), respectively, B): damage-less deposition method, C): thermal stability against the activation annealing for "gate first process".

We have already reported that low temperature divided CVD- titanium nitride (TiN) electrodes could obtain proper effective work function of 5.2eV on HfSiON keeping low leakage current by optimizing the CVD conditions, and that these divided CVD-TiN films were much promising as metal gate electrodes in p-MISFETs [4]. In this work, we found that silicon (Si) was diffused from poly-Si to high-k and that the work function shifted towards mid-gap when poly-Si films were deposited on CVD-TiN films, so we investigated the methods to suppress the diffusion of Si during poly-Si deposition.

2. Experiment

The electrical properties of TiN metal gate electrodes were evaluated with MIS capacitors. Figure 1 illustrates the structure of the MIS capacitors and the fabrication flow. HfSiON films formed by plasma nitridation of MOCVD -HfSiO were used as the dielectric layers [5]. CVD-TiN films for the gate electrode were deposited by using $TiCl_4$ and NH_3 at the relatively low temperature of 350 – 400°C by a divided deposition method in which the combination of a TiN deposition step and a post NH_3 anneal step is repeated several times [4]. Some of them were followed by the deposition of poly-Si films at 720°C. Moreover, PVD-TiN films were inserted between poly-Si and CVD-TiN films for some samples.

The contents of impurities in CVD-TiN films were detected by XPS, and the diffusions of titanium (Ti), hafnium (Hf), and Si in the stacked structure under poly-Si deposition were surveyed by SIMS depth profiles. C-V and I-V characteristics were measured using MIS capacitors, and the effective work function and EOT were calculated by using the EPOQUE program [6].

3. Results and Discussion

The dependences of the divided number of CVD-TiN on the C-V results are shown in Fig.2. The structure and the thicknesses of each layer of PVD–TiN(30nm)/CVD–TiN (10nm)/HfSiON(2nm)/Si were constant. Figures 3 and 4 show the relationship between the divided number and the composition of impurities in CVD-TiN films obtained by XPS. These indicate that as the divided number was lower, the impurities such as oxygen (O) and chlorine (Cl) increased, and also the effective work function increased from 4.9eV to 5.2eV [7].

On the other hand, for a poly-Si/CVD-TiN/HfSiON stack, a C-V curve shifted towards mid-gap direction compared to the PVD-TiN cap as shown in Fig 5. The effective work function values of these conditions were summarized in Fig. 6. With poly-Si cap, the effective work function value was shifted to 4.6eV, where the Fermi-level pinning state of a p+ poly-Si/HfSiON stack [1]. Figure 7(a) shows a SIMS depth profile of a poly-Si/CVD-TiN/HfSiON stack, where the deposition temperature of CVD-TiN was 350°C. As shown in the profile, Si atoms were diffused into TiN films, and existed at the interface between TiN/HfSiON. As a result, this Si diffusion could cause the formation of Hf-Si bonds, and Fermi-level might be pinned at the mid-gap of Si [1].

To suppress the diffusion of Si, first, we tried the increase of the deposition temperature of CVD-TiN. Figures 7(a) to (c) show SIMS depth profiles of poly-Si/CVD-TiN/ HfSiON structures, at the various deposition temperature of CVD-TiN. As the deposition temperature increases from 350 to 400 °C, the diffusions of Ti and Hf atoms were suppressed. However, the diffusion of Si was not suppressed completely, as shown in Fig 7(c). Figure 7(d) shows the SIMS depth profiles of poly-Si/PVD-TiN/CVD-TiN/ HfSiON structure. By inserting the PVD-TiN between poly-Si and CVD-TiN, the diffusion of Si, Ti, and Hf atoms were completely suppressed. These phenomena simply illustrated in Figs. 8(a) to (c). The higher temperature of CVD-TiN and the insertion of PVD-TiN were effective in controlling the diffusion of atoms.

We applied these stacks to MIS capacitors, and the C-V characteristics were shown in Figs. 9 and 10. By increasing the deposition temperature of CVD-TiN, C-V curves shifted slightly to positive bias. Moreover, by inserting the PVD-TiN films, the diffusion of Si from poly-Si to high-k was stopped completely, and the effective work function was kept at 4.9eV. Therefore, the suppression of the diffusion of Si from poly-Si to high-k could lead to the proper work functions for p-MISFETs.

4. Conclusions

We have investigated the method to control the diffusion of Si in TiN stacked metal gate electrodes during poly-Si deposition, and found that the higher temperature of CVD-TiN and the insertion of PVD-TiN were effective. PVD-TiN could prevent the diffusion of Si from poly-Si to high-k, and the proper effective work function of 4.9eV could be obtained. Therefore, the diffusion controlled TiN stacked metal gate electrodes for p-MISFETs is much potential for the next generation devices.

References

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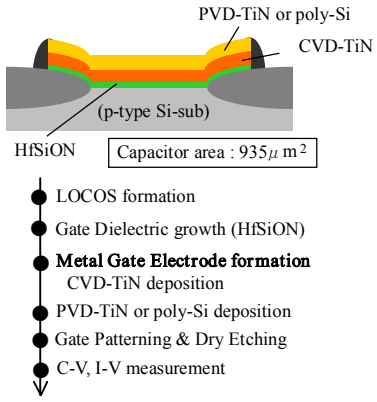

Fig. 1 MIS capacitor structure and its formation flow.

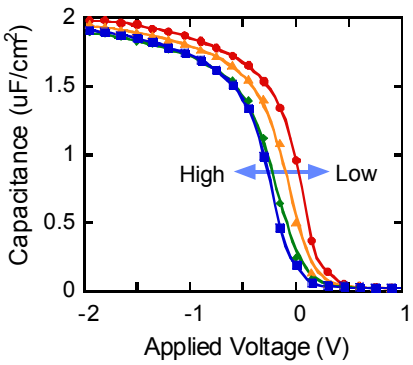

Fig. 2 C-V characteristics of divided CVD-TiN gate stacks by various conditions. Low divided number leads the effective work function high.

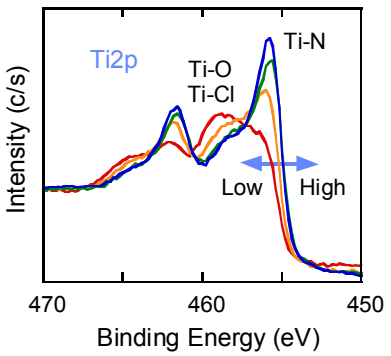

Fig. 3 Ti2p XPS spectra of divided CVD-TiN films. Ti-O and Ti-Cl bonds were shown from low divided number CVD-TiN.

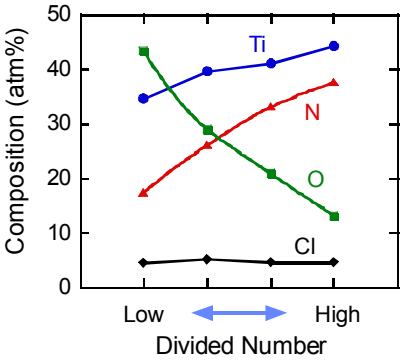

Fig. 4 Influence of divided number in a divided TiN-CVD on film composition obtained from XPS results.

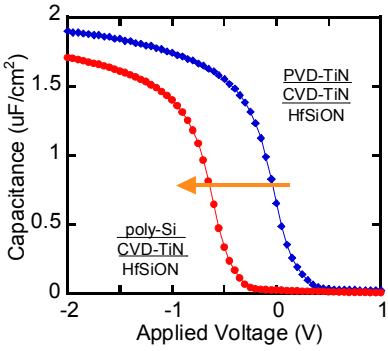

Fig. 5 C-V characteristics of CVD-TiN/ HfSiON stacks with PVD-TiN and poly-Si cap layer. CV curve shifted to mid-gap by poly-Si capping.

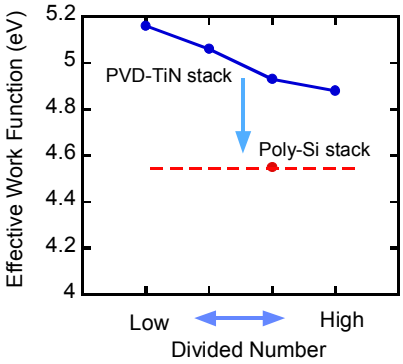

Fig. 6 Effective work function of divided CVD-TiN with PVD-TiN and poly-Si cap. By poly-Si capping, effective work function shifted to 4.6 eV.

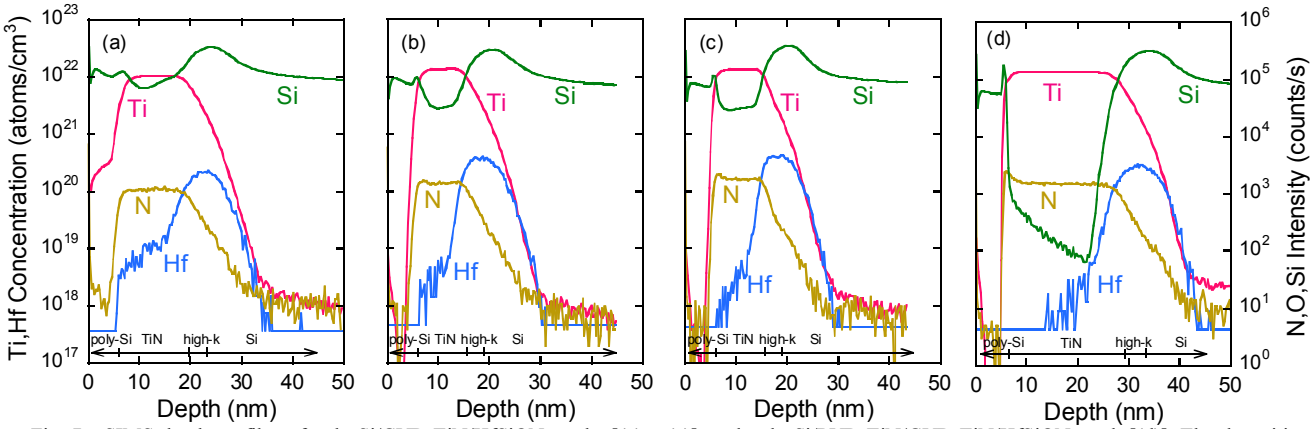

Fig. 7 SIMS depth profiles of poly-Si/CVD-TiN/HfSiON stacks [(a) – (c)], and poly-Si/PVD-TiN/CVD-TiN/HfSiON stack [(d)]. The deposition temperature of divided CVD-TiN are (a) 350°C, (b) 380°C, and (c) 400°C. by increasing the deposition temperature of CVD-TiN, the diffusion of Si, Ti, and Hf tended to decrease. By PVD-TiN capping, Si diffusion completely suppressed.

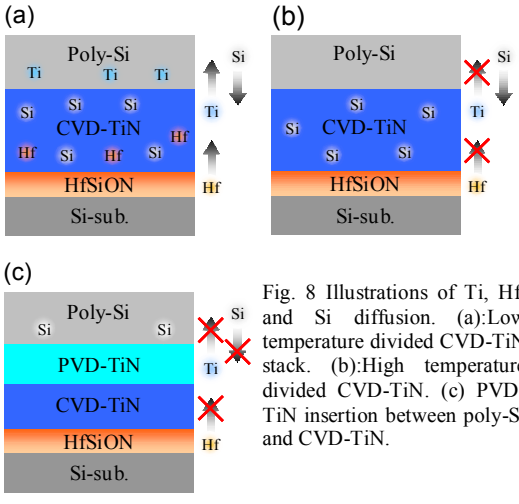

Fig. 8 Illustrations of Ti, Hf, and Si diffusion. (a):Low temperature divided CVD-TiN stack. (b):High temperature divided CVD-TiN. (c) PVD-TiN insertion between poly-Si and CVD-TiN.

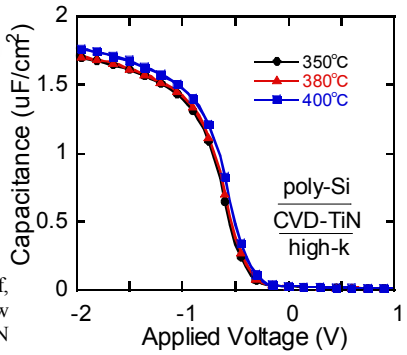

Fig. 9 C-V characteristics of poly-Si/ CVD-TiN/HfSiON stacks. CV curves slightly shifted to the positive bias with the CVD-TiN of high temperature deposition.

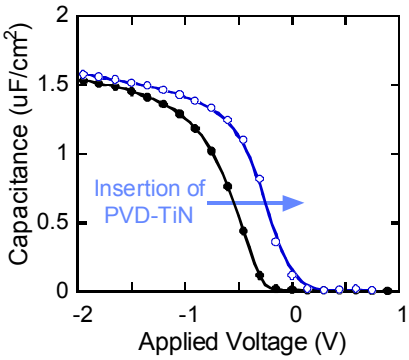

Fig. 10 Effect of insertion of PVD-TiN between poly-Si and CVD-TiN metal gate. With PVD-TiN cap, divided CVD-TiN metal gate still maintain suitable effective work function for p-MISFETs.