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Thermal stability of metal electrodes and its impact on gate dielectric characteristics

H. Park[1,4], H. C. Wen[2], M. Chang[1], M. Jo[1], R. Choi[2], B. H. Lee[2,3], S.C. Song[2], C. Y. Kang[2,4], T. Lee[4], G. Brown[2], J. C. Lee[4] and H. Hwang[1]

[1]Department of Materials Science and Engineering, Gwangju Institute of Science and Technology, Gwangju, KOREA
[2]SEMATECH, Austin, Texas, U. S. A., [3]IBM Assignee,
[4]Microelectronics Research Center, The University of Texas at Austin, Texas, U. S. A
Phone: +82-62-970-2314, Fax: +82-62-970-2304, e-mail: hwanghs@gist.ac.kr

Abstract

The effects of gate electrode materials on charge trapping and carrier mobility of metal gate devices are investigated. Devices with elemental metal and ternary metal-nitride ($M_xA_yN_z$) electrode showed higher interface and oxide trap generation than binary metal-nitride (M_xN_y) electrode devices because of electrode material diffusion into the underlying dielectric. In addition, device performance and reliability degradation of MOSFETs with ternary metal-nitride electrodes are strongly affected by electrode composition. High pressure hydrogen anneal is effective to recover interface trap density and mobility degradation caused by metal electrode.

Introduction

Metal gate electrode is needed in aggressively scaled MOSFET devices to avoid high resistance, poly depletion effect, and boron penetration caused by poly-silicon gate. Recently, numerous metals are intensively investigated to identify thermally stable band edge metals for N and PMOSFET [1].

In conventional CMOS process, high temperature annealing is required to activate source/drain dopants. While metal diffusion or reaction with gate dielectric during the high temperature process can be detrimental [2,3], their impacts on device characteristics have not been fully investigated.

In this work, trap generation behavior and carrier mobility degradation influenced by metal electrode material and its composition are discussed. In addition, the effect of high pressure hydrogen annealing on metal gate induced degradation will be investigated.

Experiment

After standard cleaning, high-k dielectric is deposited on top of chemical oxide by ALD deposition method. Various metal electrodes are deposited using PVD, CVD, ALD tools and 100nm amorphous silicon layer were deposited as a stack electrode. 1000°C anneal is used to activate source/drain implantation. Finally, conventional forming gas annealing was performed. Some samples received high pressure hydrogen annealing at 400°C for 30 minutes to enhance the interface trap passivation [4]. Process flow is summarized in figure 1. Various metal electrodes used in this study are summarized in table 1. Interface trap densities (D_{it}) are extracted using either conductance method or charge pumping method.

Results and discussion

Electrode material dependent D_{it} generation: Electron mobility of SiO_2 nMOSFET with various metal electrodes are summarized in figure 2(a). MOSFETs with ternary metal-nitride and elemental metal electrode degrade mobility, while binary metal-nitride electrodes do not show such degradation. Similar trend was observed in high-k MOSFET. To understand the mobility degradation mechanism, peak mobility (μ_{peak}) and interface trap state (N_{it}) are investigated. It is found that mobility degradation is closely related to interface trap density (figure 2(b)).

Interface trap generation mechanism is further studied using capacitors with various titanium-based metal electrodes (Ti, TiN, TiAlN, and TiSiN). CV and conductance data shows that D_{it} is strongly influenced by metal electrode species (figure 3). Ternary metal-nitrides showed more D_{it} degradation than binary metal-nitride. D_{it} degradation was more pronounced on thin SiO_2 (figure 4), suggesting some metals might have reacted with SiO_2 or diffused into SiO_2 and/or Si substrate.

To evaluate metal diffusion into Si substrate, Zerbst measurement was used and correlated with D_{it} (figure 5) [5]. Elemental Ti, Mo electrode samples exhibited shorter minority carrier generation time ($\tau_{minor.}$) and high D_{it} values, indicating Ti and Mo atoms have diffused into Si substrate. On the other hand, TiAlN and Ru electrode showed long τ_{minor} similar to the polysilicon electrode, but D_{it} was degraded, which can be explained if metal atoms diffuse into SiO_2 layer only. SIMS analysis of TiAlN and Mo are shown in figure 6 and inset respectively, supporting our observations.

Electrode composition dependent D_{it} generation: MOSFETs with ternary metal-nitride electrodes were fabricated with 3nm HfO_2. The composition of TiAlN and TiSiN are varied as in Fig.1 (b). MOSFET with Ternary metal-nitride showed significant drain current reduction(ΔI_d) during the pulse measurement, indicateing high density of oxide traps in HfO_2 layer (figure 7) [6]. Rise(fall) time varying charge pumping method shows that TaSiN with three different compositions showed higher D_{it} values than binary metal-nitride (figure 8) [7]. Wide D_{it} distribution with varying fall time indicate much higher interface states through the upper half band gap of HfO_2 in case of TaSiN. In addition, Si rich TaSiN (sample A) showed significant interface state increase at lower half band gap also. These high interface trap density can be explained by weak material binding with each electrode material and phase separation due to excess electrode material in metal electrode [8]. Since substrate hot carrier injection (SHCI) only degrades interface, SHCI can be used to find the difference at interface bonding status (figure 9) [9]. As expected, MOSFET with TaSiN electrodes showed worse V_{th} shift than binary-nitride metal electrode MOSFET. After 10^3 second SHCI stress, TaSiN electrode sample showed interface state density increase and wider trap distribution also in the upper half band gap of HfO_2. Naturally, these higher interface trap density and wider trap distribution cause significant mobility degradation.

High pressure annealing effect on D_{it} and mobility: High pressure hydrogen annealing was very effective in the passivation of the metal induced interface traps. After high pressure annealing, Humps in low frequency CV curves are eliminated and conductance loss peaks are reduced (figure 10). Dit values are also improved except Mo electrode (figure 11). Degradation in Mo sample seems to be to severe to be cured by high pressure hydrogen annealing. As shown in figure 12, mobility values are also improved by >5% and especially Si rich TaSiN showed significant improvement because of low initial mobility. As the EOT of gate stack is further scaled down and more reactive metal electrodes are used, use of high pressure hydrogen passivation process will be inevitable.

Conclusions

The effects of gate electrode materials on charge trapping and carrier mobility of metal gate devices are investigated. Binary metal-nitride electrodes showed excellent thermal stability. However, elemental metal and ternary metal-nitride electrode degraded interface trap density and in turn, mobility and hot carrier reliability. The amount of degradation is affected by the composition of ternary metal nitride system. Fortunately, metal induced interfaces states and mobility degradation could be recovered using high pressure hydrogen annealing process.

- **Wafer clean**
- **Gate dielectric growth or deposition : SiO_2 or HfO_2**
- Post Deposition Anneal(high-k)
- **Electrode deposition**
- LDD & Halo implantation
- Thin nitride layer and **poly deposition**
- Oxide spacer formation
- S/D implantation **& activation anneal**
- **Co silicide formation**
- **Pre-metal dielectric layer formation**
- **W plug with Ti/TiN liner formation**
- **Al metal pattern**
- **Post Metallization Anneal :FG anneal or HP anneal at 10atm, 400°C for 30min**

System	Ti-base electrode	Other electrode	
Unary	Ti	Poly, Ru, Mo	
Binary	TiN	TaN	
Ternary	TiSiN, TiAlN	TaSiN	A (Ta:Si:N) = 8:50:42
			B = 35:25:40
			C = 25:25:50

Fig. 1 Process flow of MOS Transistor and Capacitor (bolded processes).
Table 1. Various metal electrode used in this work. Optimum composition metal electrode used for this experiment except TaSiN electrode (number means atomic percentage).

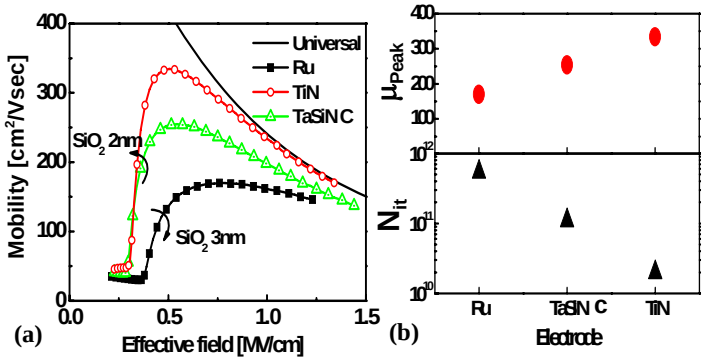


Fig. 2 Metal electrode dependent (a) mobility characteristics, (b) peak mobility and interface trap density relations. N_{it} was extracted with fixed amplitude charge pumping method at 1MHz.

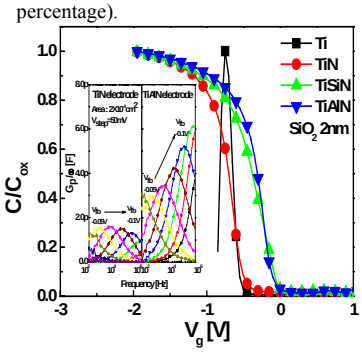


Fig.3 CV characteristics of Ti-based electrode capacitor. Inset figure shows conductance loss peak of TiN, TiAlN electrode capacitor. TiAlN showed higher interface trap densities than TiN (High G_p/w value).

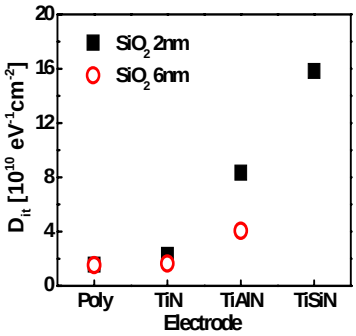


Fig.4 Electrode dependent D_{it} characteristics. Ternary metal-nitride with thin SiO_2 sample showed higher D_{it} than thicker SiO_2 and binary metal-nitride sample.

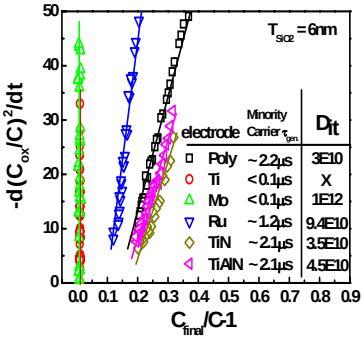


Fig.5 Zerbst plot of various electrode capacitor. Fast minority carrier generation time and significant D_{it} increase were observed in elemental metal (Ti,Mo) electrode capacitor.

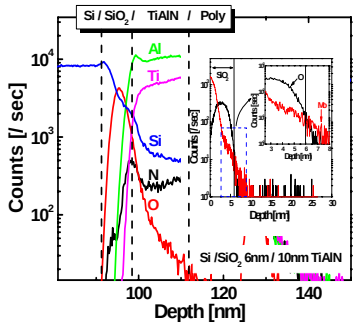


Fig.6 Backside SIMS measurement of TiAlN electrode capacitor. Metal diffused to dielectric. Inset figure shows SIMS data of Mo electrode capacitor. Clear Mo signal was observed in both dielectric and substrate.

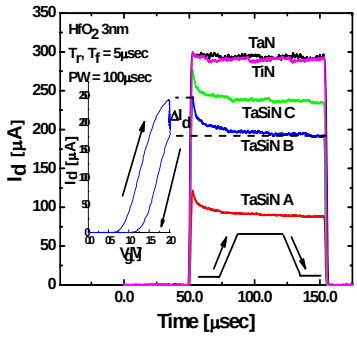


Fig.7 Metal electrode composition dependent pulsed I_d-V_g characteristics. Significant electrode material system and composition dependent I_d degradation (ΔI_d) due to charge trapping increase was observed.

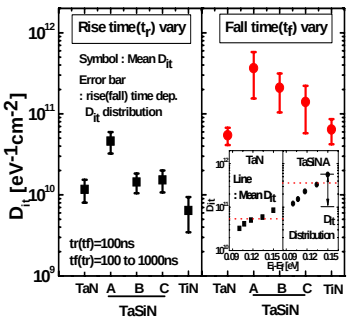
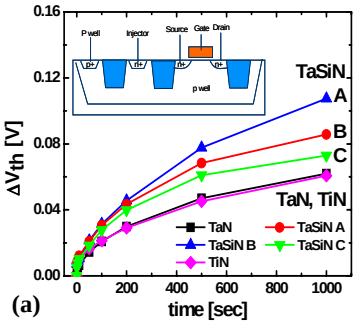


Fig.8 Metal electrode composition dependent D_{it} characteristics. D_{it} of upper and lower half band of HfO_2 was extracted with fall and rise time varying charge pumping method. Inset shows energy distribution of D_{it} from fall time varying charge pumping measurement.



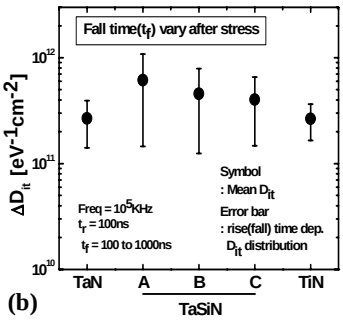


Fig.9 (a) Threshold voltage shift under substrate hot carrier stress (E_{ox}=3.5MV/cm^2, $V_{injector}$=-5V, V_{body}=-4V). Inset figure shows schematic diagram of substrate hot carrier transistor with n+ injector.
(b) D_{it} characteristics of upper half band of HfO_2 after 10^3 second substrate hot carrier stress. Strong fall time dependent D_{it} variation was observed after stress.

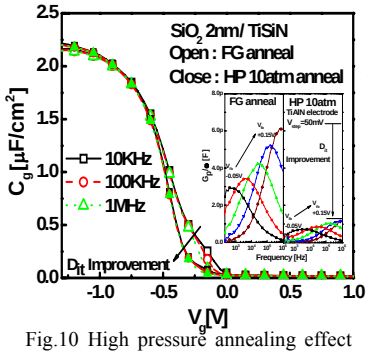


Fig.10 High pressure annealing effect on TiSiN electrode capacitor. Significant improvement of CV characteristic was observed.

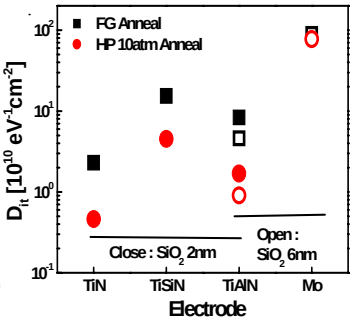


Fig.11 High pressure annealing effect on various metal electrode capacitors. Metal impinged into Si sample (MO) shows no D_{it} improvement.

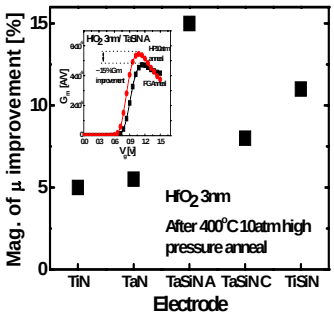


Fig.12 Summary of mobility improvement after high pressure annealing. Inset shows transconductance improvement after 10atm high pressure anneal.

Refernces

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Acknowledgement

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