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Pd_2Si Fully-Silicided Gate: Kinetics of Silicide Formation and Workfunction Tuning

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1. Introduction

NiSi fully-silicided (FUSI) gate is one of the most promising candidates for metal gate CMOS technology [1] because of its process compatibility and workfunction tunability by predoping [2,3]. Dopant pileup formed by snowplow effect [4] during silicidation is considered to be the origin of workfunction shift. However, the reported magnitude of the shift was insufficient for CMOS application [5-8], and a detail of workfunction shift mechanism is still unclear. In addition, an adhesion issue of doped NiSi film and void formation at the $NiSi/SiO_2$ interface was pointed out [7-9]. Research on the other silicides would help better understanding and improving FUSI gate technology.

We have investigated Pd_2Si FUSI gate MOS structure. Pd_2Si has higher thermal stability than NiSi [10], and its lower silicidation temperature provides flexibility for device fabrication process. Residual compressive stress in a Pd_2Si film is 50 MPa [11], which is much smaller than NiSi (720 MPa) [12]. These stress values might be related to the volumetric changes due to silicidation. Since the snowplow effect similar to NiSi was reported for Pd_2Si [4], workfunction tunability is also expected. In this report, Pd_2Si FUSI gate formation process and workfunction tuning are described.

2. Pd_2Si FUSI gate Formation

Fig. 1 shows the fabrication process flow of Pd_2Si FUSI gate MOS diodes. Since Pd_2Si is the first phase in a Pd-Si system, one step annealing was performed for silicidation. Three types of heating equipments, lamp heating in a sputtering chamber, hot-plate and RTA were used for silicidation. Fig. 2 shows XTEM (cross-sectional TEM) image of Pd_2Si FUSI gate formed at 250 °C with lamp heating. Needle-like silicide growth at the surface, formation of mixed silicide phases and void formation at the Pd_2Si/SiO_2 interface were observed. In the case of hot-plate heating, only the Pd_2Si phase was formed, which was confirmed by X-ray diffraction [13]. This is attributed to higher ramp-up rate because of large thermal capacity ratio of the hot-plate and a Si substrate. However, the voids at the interface were still formed at 250 °C even with the hot-plate heating especially for the predoped case shown in Fig. 3(a). This void formation was avoided by raising the silicidation temperature to 300 °C (Fig. 3(b)). Similar results were obtained by the RTA silicidation. These results indicate that the ramp-up rate for silicidation annealing as well as the silicidation temperature and the presence of impurities are key factors to control the silicide formation, as illustrated in Fig. 4. Since an excessive Si diffusion toward the NiSi surface and the resulting void formation have also been found in Sb doped NiSi FUSI gate [14], the reduction of Si diffusion is a common issue for FUSI gates.

3. Workfunction Tuning by Impurity Predoping

As shown in Fig. 5, the workfunction of undoped Pd_2Si FUSI gate was estimated to be 4.57 eV. Fig. 6 shows C-V characteristics for undoped and P, As, and Sb predoped Pd_2Si FUSI gate MOS diodes. The positive flatband voltage (V_{FB}) shifts were obtained with these impurities inspite of n-type dopants. The maximum V_{FB} shift obtained with P was +0.25 V regardless of the implantation dose. No interfacial layer formation was found in the XTEM image as shown in Fig. 7. From EDX analysis, P signal was detected only in the Pd_2Si layer in the vicinity of the Pd_2Si/SiO_2 interface. These results indicate that impurity pileup at the interface is an origin of the workfunction shift, as in the case of NiSi. On the other hand, the V_{FB} shift of -0.30 V was obtained for BF_2 predoped Pd_2Si, as shown in Fig. 8. Furthermore, the V_{FB} shift of +0.30 V was obtained with F predoping, despite no shift in NiSi [7,8]. It is interesting that the Pd_2Si FUSI gate workfunction shifts by As, P, Sb and BF_2 predoping are all in the opposite direction to the NiSi [5-9] and PtSi [15], as summarized in Fig. 9.

4. Summary

It has been found that the high ramp-up rate to avoid the silicidation reaction at low temperature is an important factor to control the quality of the silicide layers. The workfunction of undoped Pd_2Si is 4.57 eV, which can be modulated by impurity predoping of poly-Si. It is noteworthy that the Pd_2Si workfunction shifts with various impurities are all in the opposite direction to the NiSi case.

Acknowledgement

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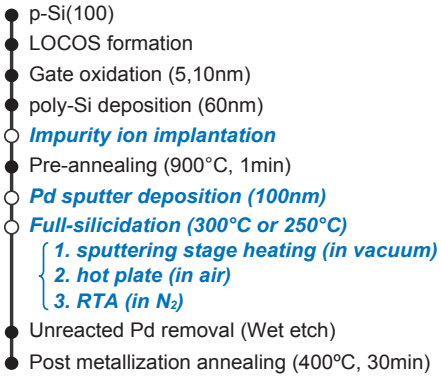


Fig. 1 Fabrication process flow of Pd_2Si FUSI gate MOS diodes.

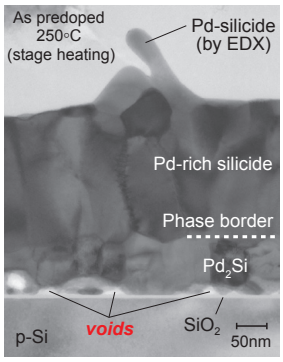


Fig. 2 XTEM image of As predoped Pd_2Si FUSI gate formed at 250 °C with lamp heating. Initial Pd and poly-Si thicknesses were 180 nm and 100 nm, respectively.

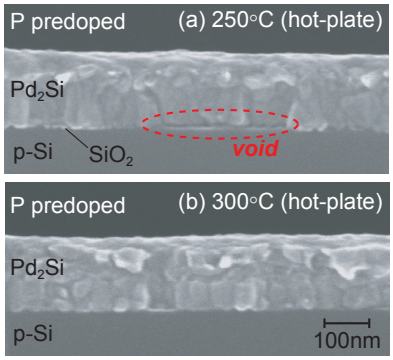


Fig. 3 Cross-sectional SEM micrograph of Pd_2Si FUSI gate formed at 250 °C (a) and 300 °C (b) with hot-plate heating.

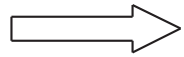
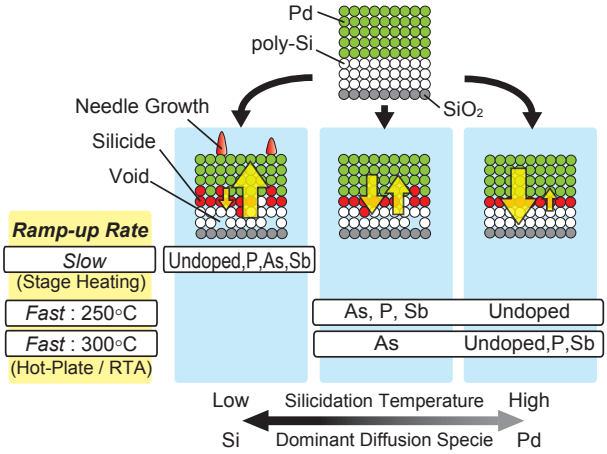


Fig. 4 Schematic model of silicide formation under various silicidation conditions. Silicidation temperature, its ramp-up rate and the presence of impurities affect the kinetics of silicide formation due to the change of dominant diffusion species.



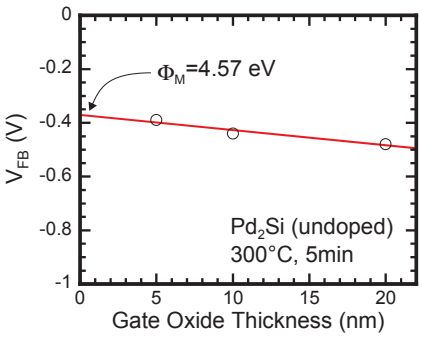


Fig. 5 Flatband voltage as a function of gate oxide thickness extracted from the C-V characteristics of undoped Pd_2Si FUSI gate MOS diodes.

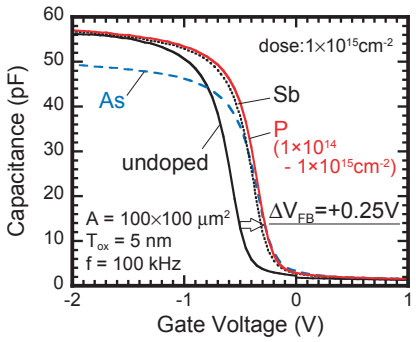


Fig. 6 C-V characteritstics of Pd_2Si FUSI gate MOS diodes with As, P or Sb doping. V_{FB} shift of +0.25 V was obtained with P predoping regardless of implanted dose. Capacitance reduction due to void formation occured with As doping.

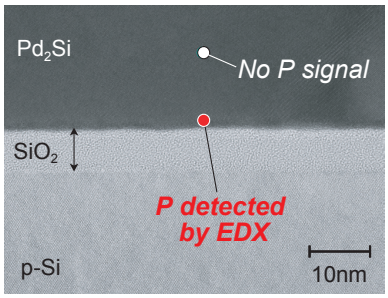


Fig. 7 XTEM image of the interfaces in P predoped Pd_2Si FUSI gate MOS diode. P signal was detected at the Pd_2Si/SiO_2 interface by EDX analysis.

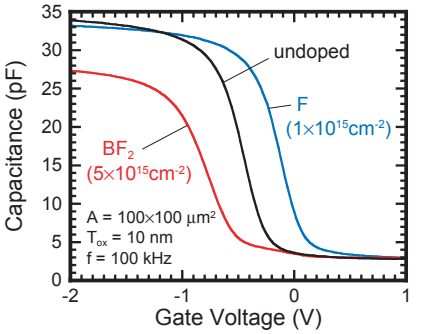


Fig. 8 C-V characteritstics of Pd_2Si FUSI gate MOS diodes with BF_2 or F. V_{FB} shift of -0.3 V and +0.3 V were obtained with BF_2 and F predoping, respectively.

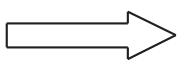


Fig. 9 Summary of the workfunction shift with various impurities in NiSi [5-8], PtSi [15] and Pd_2Si FUSI gate MOS structures. The range of workfunction values of Pd_2Si (~0.6 eV) is comparable to that for NiSi, but the shifts in Pd_2Si are all in the opposite direction to the NiSi and PtSi.