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# Workfunction Adjustment Using Thin Metal Film (Ti, Pd) under FUSI Gate Electrode and Laser Annealing

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## 1. Abstract

We demonstrate a scheme of fabricating fully silicided (FUSI) gate electrode with workfunction (WF) ranging form 4.05eV to 5.14eV. A thin metal film, either Ti or Pd (~2-10nm) is deposited on the gate insulator ($SiO_2$ & high-*k*) prior to depositing FUSI materials (Ni & Si). It results in a metal rich mixed phase of the thin film metal at the gate/insulator and NiSi as top gate after rapid thermal annealing. By controlling the Ti or Pd film thickness, the gate controlled WF shifts towards the conduction or valance band edge. The WF resulted is stable and free from Fermi-level pinning. In addition, coupled with the aid of laser annealing, the composition of the metal rich phase at the interface can be further altered and fine-tuned, hence resulting in a robust control of WF over the range of interest.

## 2. Introduction

Workfunction (WF) engineering for metal gate has been under intense research due to its critical importance in device performance. Fully silicided(FUSI) gate electrode is one of the promising candidates for metal gate technology[1,2]. Possible ways to tune the WF in FUSI gate include the dopant segregation effect, $Ni_xSi_y$ phase effect, Ni alloy etc. However, each method is not able to give wide range WF, especially for NMOS gate electrodes, and possibly with adverse effects[3]. These effects, however, have drawn attention to the gate/insulator interface and confirmed its role in the gate WF. Our work focuses on the role of interface engineering; the WF determining elements were incorporated prior to poly-Si deposition instead of putting them last.

## 3. Experiments, Results, and Discussion

Ti or Pd (2to10nm), Ni (30nm), and Si (40nm) were sequentially sputtered onto gate dielectric using physical vapor deposition (PVD). Rapid thermal annealing (RTA) at 400°C was carried out to form FUSI. The schematic structures upon deposition and after RTA are shown in Fig.1, respectively. Fig.2(a) shows XTEM of a formed structure. They were then patterned to form MOS structure and the corresponding WF was extracted with CV measurements. Both thermally grown $SiO_2$(1.6-20nm) and $HfO_2$(4-16nm) /$SiO_2$(7Å) (EOT=20-43Å) were used as gate dielectric. Besides using the amorphous Si-last FUSI process, the normal NiSi FUSI samples formed using poly-Si first process and without the Ti/Pd interfacial layer were also prepared for comparison.

***a) Basic findings:*** The apparent shift in WF is shown in the CV (Fig.3) and the values of WFs extracted are shown in Fig.4. The samples without the interfacial layer (i.e. Ni+α-Si) shows a similar WF as the normal NiSi FUSI control samples, indicating that the sequence of Ni and Si deposition and the phase of Si upon deposition do not affect the final WF. This confirms the shift in the WF is due to the presence of Ti or Pd at the gate/insulator interface. Fig.5 shows that prolonged annealing and/or annealing at a higher temperature does not change the WF, confirming that the resulted structure is thermally stable with excellent gate leakage characteristics (Fig.6).

***b) Material analysis:*** TEM/EDX (Fig.2(b)) shows a Ti-rich NiSi layer close to the interface. SIMS analysis (Fig.7) shows the element distribution in the gate. NiSi and Ti inter-diffusion starts to occur, with Ti concentration peaked at the gate/insulator interface. With XPS analysis shown in Fig.8, Ti at the interface is found to remain as elemental Ti as Ti is expected to be inert with Si or $SiO_2$ at 400°C[4,5].

***c) WF vs. the as-deposited metal film (Ti, Pd) thicknesses:*** By varying Ti/Pd film thickness, the WF can be further tuned towards the conduction/valence band edge (Fig.9). This is attributed to the increasing Ti/Pd concentration in the interfacial metal layer, proven by SIMS in Fig.7. The same effect is seen on high-k samples, and an absence of Fermi-level pinning effect. The smaller range of WFs obtained is probably due to the stronger surface dipole[6]. WF of values spanning the whole silicon bandgap can be obtained by this mechanism, as summarized in Fig.10.

***d) Robust fine-tuning of WF by laser thermal annealing:*** We further developed a technique to provide WF fine-tuning with a 248nm KrF excimer laser. With Ti as interfacial layer (3nm), WF starts to shift towards the valence band with laser fluence greater than 0.1J/cm$^2$. Higher fluence brings more WF shifting (Fig.11). When multiple pulses are used, the first pulse shows the greatest impact, and the subsequent pulses provide the required fine-tuning with a precision of 0.02eV(Fig.12). The thermal energy generated by laser has probably induced chemical redistribution of metal at the gate/insulator interface, where Ti concentration dropped as a consequence. Degradation in CV can be avoided if laser fluence of ≤0.3J/cm$^2$ is used, as shown in Fig.11. This technique can potentially be used to fine-tune WF of p and nMOS separately by localized laser annealing with anti-reflection coating of p or nMOS.

***e) Proposed mechanism and model:*** Ti, Pd thin film deposited at the gate/insulator interface diffuses into NiSi during RTA and results in a *stable* metal-rich mixed phase of probably Ti or Pd and NiSi. The chemical composition close to the gate/insulator interface is critical to the gate WF. Hence, a high concentration of Ti/Pd brings WF to their elemental WF on $SiO_2$ (3.9&5.22eV), as seen in Fig.10.

## 4. Conclusions

We have demonstrated a novel process and a proposed mechanism for fabricating FUSI gate electrode with wide WF tuning range (4.05-5.14eV). With localized laser annealing, WF can be fine-tuned with a precision of 0.02eV.

## References

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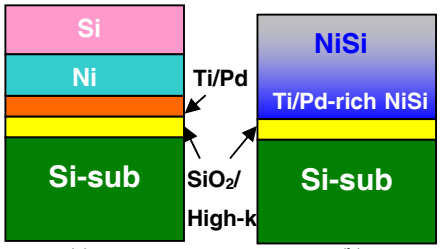


Fig.1. Schematic illustrations of MOS structure (a) upon deposition, (b) after RTA.

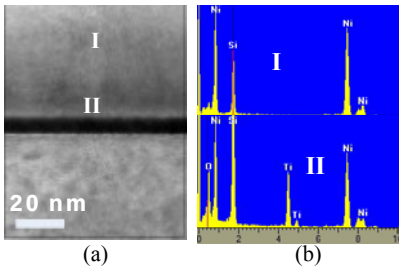


Fig.2. (a) XTEM showing the MOS structure formed from an as-deposited structure: Si(40nm)/Ni(30nm)/Ti(3nm)/$HfO_2$(9nm)/$SiO_2$(7Å)/Si, (b) TEM/EDX analysis at the top gate and the gate/insulator interface.

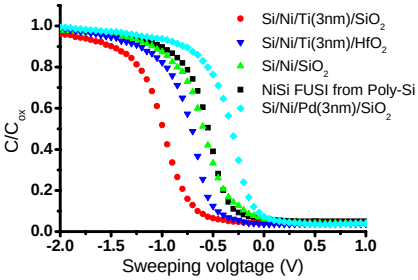


Fig.3. Capacitance vs. voltage curve showing the WF shifts in different MOS structures.

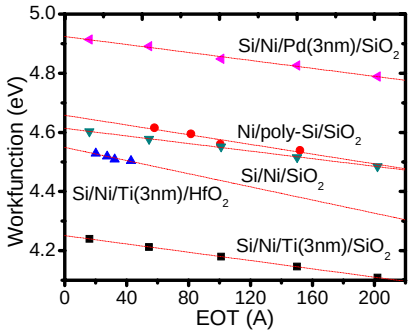


Fig.4. Extracted WF from CV curve showing the effect of the interfacial Ti/Pd layer.

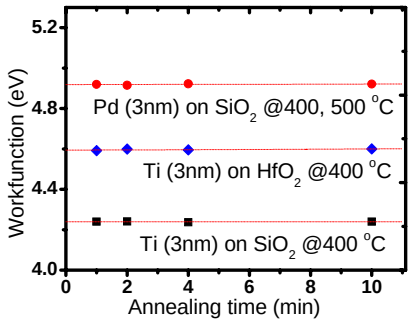


Fig.5. Prolonged annealing showing no effect on the WF, proving the thermal stability.

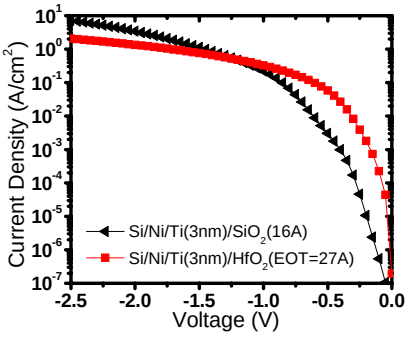


Fig.6. Leakage current density of gate with 3nm Ti as interfacial layer on $HfO_2$ and $SiO_2$.

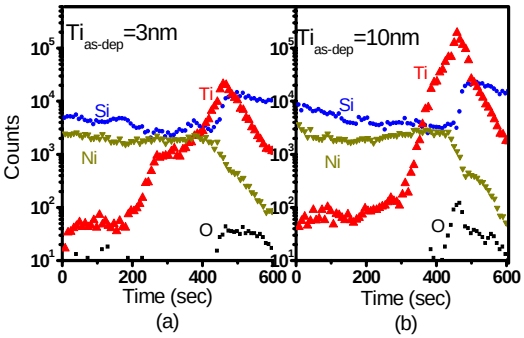


Fig.7. SIMS analysis shows inter-diffusion of Ti and NiSi, with Ti concentration peaked at gate/insulator interface. (a)$T_{as\_dep}$=3nm, (b) $T_{as\_dep}$=10nm.

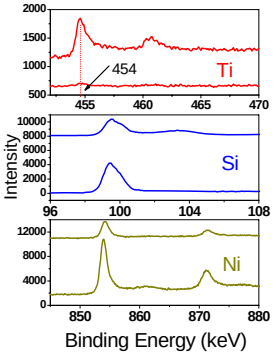


Fig.8. XPS analysis at the gate/insulator interface (top curve) and 1/2 of total FUSI thickness (bottom curve).

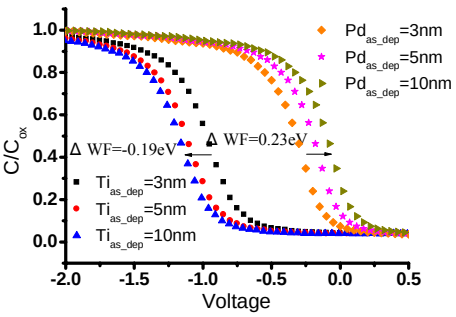


Fig.9. CV characteristics showing the shifts in WF by changing the as-deposited metal film (Ti, Pd) thickness.

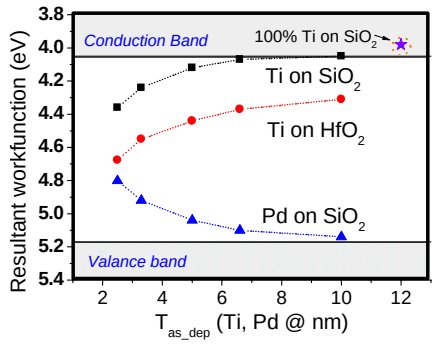


Fig.10. WF range obtainable by changing the as-deposited metal film (Ti, Pd) thickness on both $SiO_2$ and $HfO_2$.

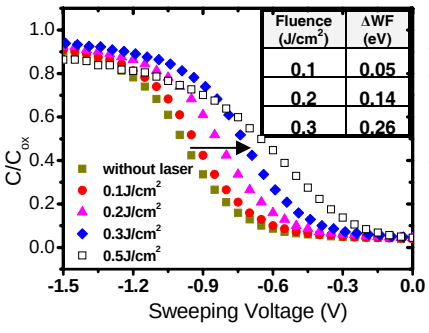


Fig.11. CV characteristics showing the effect of laser thermal annealing on WF. Single laser pulse is operated on Ti samples for each fluence level.

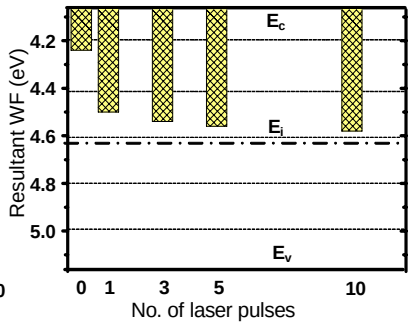


Fig.12. WF fine tuning by applying multiple laser pulses, with the same fluence level at 0.3 J/cm$^2$.