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Mechanism of Threshold Voltage Reduction and Hole Mobility Enhancement in pMOSFETs Employing Sub-1nm EOT HfSiON by Use of Substrate Fluorine Ion Implantation

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1. Introduction

One of the most serious drawbacks in CMOS devices with Hf-based high-k gate dielectrics is the extremely high threshold voltage (V_{th}) of the p+poly-Si gate pMOSFET [1]. Even using the metal gate electrodes with a high vacuum work function, such as Ru, Pt and Re, it is difficult to obtain a high effective work function when combined with Hf based high-k gate dielectrics [2]. Although it has been proposed that aluminum content control in HfAlOx can provide symmetrical V_{th} values for nMOS and pMOS [3], low carrier mobility in MOSFETs with ultra-thin EOT $HfAlO_x$ remains a serious issue. Recently, it has been reported that fluorine incorporation in HfSiON by F ion implantation into the silicon substrate before HfSiON formation provides an effective method to reduce the V_{th} of p+poly-Si gate pMOSFETs [4,5]. However, its validity for, and influence on sub-1nm EOT HfSiON have not yet been clarified. The mechanism of the reduction in V_{th} also appears to be not yet well understood. This paper reports the evaluation of the impact of ion implanted F on hole mobility, as well as the effect on V_{th} reduction, in pMOS employing sub-1nm EOT HfSiON gate dielectrics. In addition, the mechanisms of the V_{th} reduction and hole mobility improvement have been investigated.

2. Experimental

Figure 1 shows the fabrication process flow for HfSiON gate dielectrics with substrate F ion implantation. F^+ I/I through a 2 nm sacrificial SiO_2 layer with an ion energy of 8.0 or 17 keV at 7° was performed either before or after well/channel activation annealing. Ultra-thin HfSiON was fabricated using MOCVD HfSiO, followed by plasma nitridation and a high-temperature post-nitridation annealing processes [6]. The EOT of the HfSiON gate dielectrics used in this work was 0.98 nm. Using the HfSiON gate dielectrics, poly-Si gate pMOS and nMOS were fabricated from a conventional CMOS process with spike anneal S/D activation at 1030°C. X-ray photoelectron spectroscopy and positron annihilation were used to evaluate charge build-up in the HfSiON film and defects in the silicon substrate, respectively. A process and device simulator, ENEXSS [7], was used to fit the obtained C-V characteristics and to calculate the electric field and the hole density in the inversion layer of the pMOSFET.

3. Results and Discussions

In order to efficiently introduce F atoms into Si substrate, the energy of F^+ ions should be 8.0 keV or above. In the case of F^+ I/I before well/channel anneal, most of the implanted F atoms diffuse out from the surface during the anneal, and the residual quantity has a maximum value of about 3%, using 8.0 keV. We have fixed the ion energy at 8.0 keV for the F^+ I/I before the anneal and at either 8.0 or 17 keV for the F^+ I/I after the anneal, in order to evaluate the effects of the ion energy and the timing of implantation with the same dosage.

Figure 2 shows C-V characteristics of p+poly-Si gate pMOSs with various fluorine implant doses. F implantation renders the slope of the increase in C_g from depletion to inversion more gentle and that from depletion to accumulation steeper. Corresponding to this distortion of C-V curves, the I_d-V_g characteristics of the pMOS shift in the positive direction (Fig. 3). V_{th} in p+poly-Si gate pMOS with sub-1nm EOT HfSiON can be markedly reduced by the F^+ I/I, as summarized in Fig. 4. The V_{th} reduction shows a linear dependence on F dose and its reduction by as much as 250 mV was achieved with a $1x10^{15}$ cm^{-2} at 17 keV,. Greater V_{th} shifts were obtained at the higher ion energy, although the timing of implantation does not affect the extent of V_{th} shift. In addition to the V_{th} reductions, hole mobility is notably increased with increasing F dose, as shown in Fig. 5. The hole mobility also shows linear dependence on the F dose, as shown in Fig. 6. The extent of mobility increase does not depend on the ion energy and depends on the timing of implantation. The mobility enhancement has been obtained up to about 30% at surface carrier concentration, N_s, of $1x10^{13}$ cm^{-2} for a $1x10^{15}$ cm^{-2} F implant at 17 keV. To understand dependence of V_{th} shift and mobility enhancement on the ion energy and the timing, the mechanism still needs to be clarified.

Since the V_{th} shifts in n+poly-Si gate pMOSFETs were same as those in p+poly-Si gate pMOSFETs, the origin of the V_{th} reduction is thought to reside below the gate electrode/dielectric interface. As illustrated in Fig. 7, three possible models, namely, negative fixed charge in insulator, acceptor type interface states and negative charge in Si-substrate, were considered. The first of these can explain a simple parallel shift in C-V curves, but cannot explain the distortion of the C-V curves shown in Fig. 2. The second should bring about a negative charging in an insulating layer. However, the Hf_{4f} spectrum obtained from the F implanted sample shows a binding energy shift in the positive direction, which can be explained by positive charge in insulator or increase in the Fermi level of the Si surface (Fig. 8). The *S*-parameter in Si-substrate obtained from positron annihilation was decreased by the F^+ I/I and HfSiON formation, which suggests the existence of fluorine-vacancy complex defects in the Si-substrate [8]. The decrease in S-parameter was noted for the positrons with sufficiently high energy to penetrate the F implanted region, which is explained by the existence of attractive forces for positrons, i.e., the existence of negative charges. This supports the validity of the third model. Fluorine atoms implanted into Si substrate tend to diffuse out from surface during the following annealing steps. Therefore, the negative charges are thought to be located in the surface region of the Si substrate. In fact, the placement of negative charges (acceptors) shown in Fig. 10 can precisely reproduce the changes in C-V curves, as shown in Fig. 11. These charge distributions decrease the electric field in surface region of inversion layer (Fig. 12) and hence the distance between the carriers and interface tends to be large (Fig. 13). This is thought to be qualitatively consistent with the observed hole mobility enhancement. Further investigation to characterize the fluorine related defects and to clarify the kinetics will provide a quantitative explanation for the benefit of this process.

4. Conclusion

Fluorine implantation into the channel region before formation of gate dielectrics has been found to be an effective method by which to reduce the V_{th} and enhance the hole mobility in pMOS devices with ultra-thin HfSiON. V_{th} reduction of up to 250 mV was obtained and approximately 30% in hole mobility enhancement at N_s=$1x10^{13}$ cm^{-2} was achieved for a $1x10^{15}$ cm^{-2} implant at 17 keV. Both the V_{th} reduction and the hole mobility enhancement are thought to be due to F induced negative charges, which are automatically localized in the shallow region at the Si surface.

References

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○ **STI formation**
○ **sacrificial oxidation (2 nm)**
○ **well/channel doping**
○ ***w/ or w/o F⁺ I/I (8.0 keV, 7º)***
○ **well/channel annealing (850ºC, 30 s)**
○ ***w/ or w/o F⁺ I/I (8.0 or 17 keV, 7º)***
○ **sacrificial SiO_2 removal**
○ **IFL (0.7 nm) formation (250ºC)**
○ **HfSiO deposition (260ºC)**
○ **plasma nitridation (200ºC)**
○ **post-nitridation annealing (PNA) (1050ºC, 5 s, 0.1% O_2)**

Fig.1 Process flow of ultra-thin HfSiON gate dielectrics with substrate fluorine implantation. EOT of HfSiON used in this work was 0.98nm.

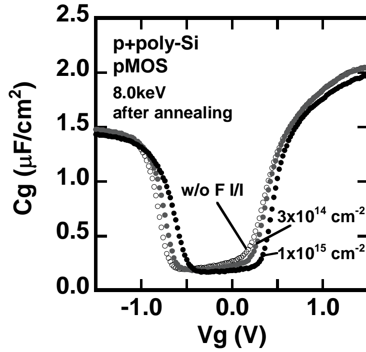

Fig.2 C-V changes in p+poly-Si gate pMOS due to F^+ I/I (8.0 keV, 7º, $3x10^{14}$ and $1x10^{15}$ cm^{-2}). F^+ I/I was performed after well/channel anneal.

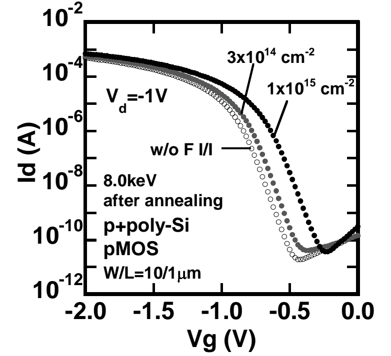

Fig.3 I_d-V_g changes due to F^+ I/I (8.0 keV, 7º, $3x10^{14}$ and $1x10^{15}$ cm^{-2}). F^+ I/I was performed after well/channel anneal.

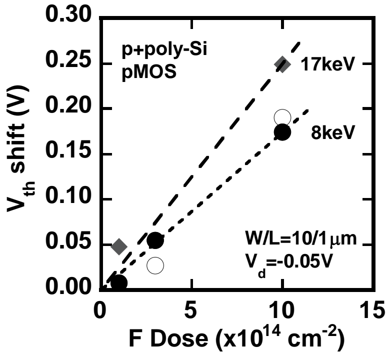

Fig.4 Dependence of V_{th} shifts in pMOS on F dose. Open symbol indicates F^+ I/I before anneal. High energy results in larger V_{th} shifts.

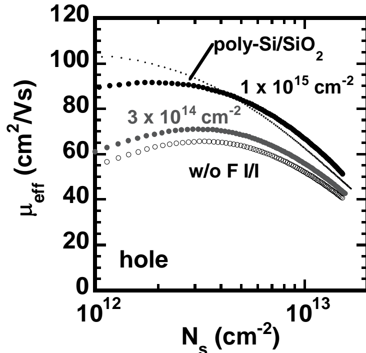

Fig.5 Effective hole mobility in p+poly-Si pMOS vs surface carrier density. F^+ I/I was performed after well/channel anneal.

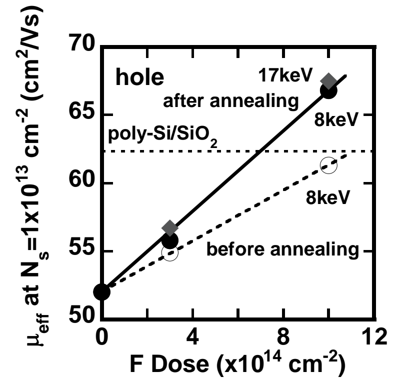

Fig.6 Dependence of effective hole mobility at N_s=$1x10^{13}$ cm^{-2} in p+poly-Si pMOS on F dose. F+ I/I before anneal shows smaller μ_{eff} increase.

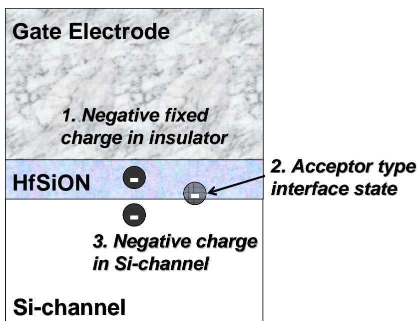

Fig.7 Possible models of V_{th} reduction in F^+ implanted pMOSFETs.

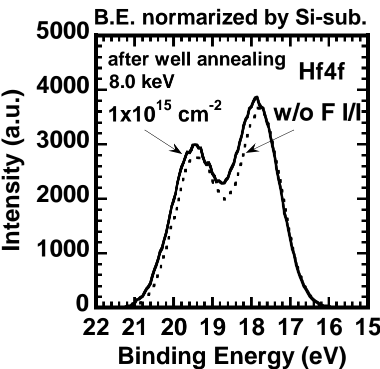

Fig.8 Hf_{4f} photoelectron spectra obtained from HfSiON films w/ or w/o F I/I. Binding energy was normalized to Si_{2p}(Sub.)=99.3eV.

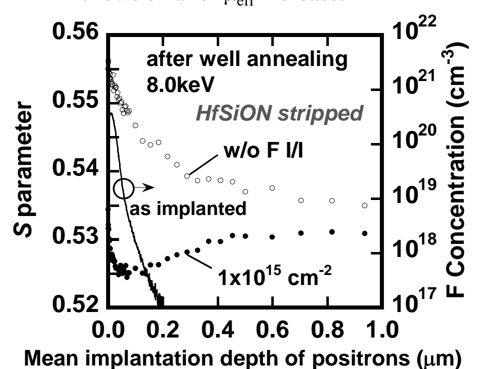

Fig.9 Mean implantation depth dependence of *S* parameters of positron annihilation in Si substrates, w/ or w/o F I/I.

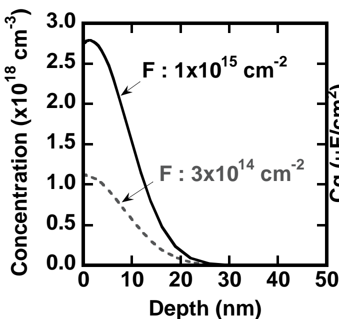

Fig.10 Additional acceptor profiles, which fit C-V characteristics of F^+ implanted pMOSFETs.

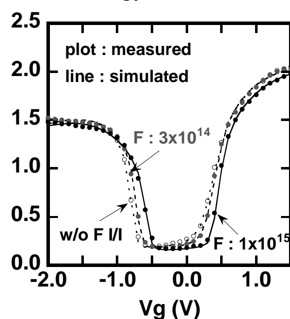

Fig.11 Simulated C-V characteristics of pMOSFETs, w/ or w/o F I/I.

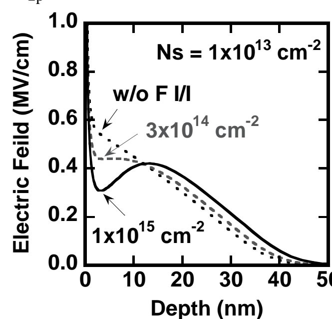

Fig.12 Depth profiles of calculated electric field in inversion layer of pMOSFETs, w/ or w/o F I/I. (N_s=$1x10^{13}$ cm^{-2})

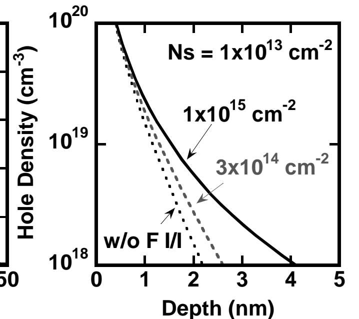

Fig.13 Calculated hole density in the surface region in the inversion layer of pMOSFETs, w/ or w/o F I/I.