Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Yokohama, 2006, pp. 398-399

J-6-2

Fabrication of SiO_2/Ge MIS structures by plasma oxidation of ultrathin Si films grown on Ge

Hiroshi Kumagai[1], Masato Shichijo[1], Hiroto Ishikawa[1], Takuya Hoshii[1], Satoshi Sugahara[1], Yasutaka Uchida[2], and Shinichi Takagi[1]

[1]Graduate School of Frontier Science, The Univ. of Tokyo
7-3-1 Hongo, Bunkyo-ku, Tokyo 113-8656, Japan
Phone & Fax : +81-3-5841-6733, e-mail : kumagai@mosfet.k.u-tokyo.ac.jp
[2]Teikyo University of Science and Technology
2525 Yatsuzawa, Uenohara-shi, Yamanashi 409-0193, Japan

1. Introduction

As the continued scaling of Si CMOS devices approaches its fundamental limits, a variety of technology boosters including the improvement of channel mobility are being investigated to increase the saturation current. From this viewpoint, Ge channels attract an interest because it offers higher mobility than Si (2x for electrons and 4x for holes). The most critical issue on Ge MOSFETs has been recognized as the realization of the good MOS interfaces. In spite of the many attempts, however, the gate insulator formation technologies on Ge have not been established yet. On the other hand, it has recently been reported that SiO_2/SiGe MIS structures formed by the Ge-condensation method provide the hole mobility of 10 times as high as the universal one [1]. Also, ultrathin Si interlayers between Ge and dielectrics have been reported to be effective in reducing N_{ss} and the C-V hysteresis. [2] These results suggest that the Ge surfaces terminated with SiO_2 or Si atomic layers can exhibit high quality interface properties.

In this paper, we propose a novel technique to fabricate SiO_2/Ge MIS structures, where ultrathin Si films epitaxially grown on Ge substrates are oxidized at low temperatures by O_2 plasma oxidation. Here, one possible advantage of this technique is the potentiality to precisely control the MIS interface structures by adjusting oxidation time. The physical and the electrical properties of the MIS structures fabricated by this technique are presented.

2. Samples Fabrication

The fabrication flow is shown in Fig. 1. SiO_2/Ge MIS capacitors were fabricated on (100) oriented n- and p-type Ge substrates. Cyclic HF (buffered HF) dip with DI water was used to remove Ge native oxides. Si films of as thin as 1.2-1.5 nm were grown at 100 °C by MBE. Subsequently, the samples were oxidized at 200 °C in O_2 plasma for 60, 90, and 120min. Finally, Al films were deposited to form gate electrodes.

3. Results and Discussions

Fig. 2 shows the SiO_2 (Ge oxide) thickness formed by plasma oxidation of Si substrates, Si films on Ge and Ge substrates as a function of the oxidation time. It is found that the SiO_2 thickness on Ge is thinner than that on Si substrates and Ge oxides on Ge substrates. Actually, the thickness of SiO_2 on Ge is almost determined by the initial Si film thickness. These results mean that the oxidation rate of Ge beneath SiO_2 is much slower than that of Ge substrates. Fig. 3 shows a TEM image of a SiO_2/Ge structure oxidized in O_2 plasma for 60min. It is found that SiO_2 with uniform thickness and almost flat interface is realized. This result indicates the advantage of MBE, allowing us to form uniform Si films directly on Ge at a low temperature of 100 °C, applicable to ultrathin Ge-On- Insulator substrates, as well.

XPS analyses were performed to study the MOS interface properties. It is observed from the Si 2p spectrum of the samples oxidized for 60min (Fig. 4) that a Si peak is hardly observed, compared with the large SiO_2 peak, meaning that the Si films was fully oxidized. As for the Ge 3d spectrum, a small peak of GeO_2 is observed in addition to the peak of Ge substrates (Fig. 5), suggesting that the Ge substrates was also oxidized. It is also found in the oxidation time dependence (Fig. 6) that the peak energy, corresponding to GeO_2, does not change and the peak height increases with an increase in the oxidation time. As a result, we can estimate that the fabricated MIS capacitors are composed of SiO_2/GeO_2/Ge layered structures, independent of the oxidation time.

Fig. 7 show the C-V characteristics of capacitors on n- and p-type substrates, respectively. The observed large change in the capacitance suggests the modulation of the surface potential, while the large frequency dispersion, attributable to high intrinsic carrier concentration of Ge [3], is observed. Also, the C-V curves do not depend on the oxidation time (Fig. 8), indicating that the electrical properties at the MIS interfaces are determined by GeO_2/Ge interfaces. In order to obtain high-frequency C-V curves, the C-V measurement at 1 MHz was performed at lower temperatures (Fig. 9). It is found that the slope of C-V becomes steeper and C_{min} becomes lower with decreasing the temperature. As a result, the C-V curves at -50°C can be regarded as in the high frequency limit, while the C-V data at higher temperatures can include the response of interface states and minority carriers even at 1 MHz. Fig. 10 shows the energy distribution of N_{ss} estimated by the Terman method using the C-V curve at -50°C. The U-shape distribution is observed, as similar with Si MOS interfaces. The minimum value of N_{ss} is estimated to be in the order of 10^{11} $eV^{-1}cm^{-2}$. The N_2 and forming gas (7% H_2) anneals after metal gate formation (PMA) were carried out at 300°C for 30 min to aim at improving the interface properties. As shown in Fig. 11, however, the dispersion of C-V curve and the slope is almost the same and the flat band shift toward the positive gate voltage is observed, indicating little improvement in N_{ss} and the generation of negative fixed charges. As a result, forming gas anneal seems not to be effective in improving the interface properties of SiO_2/GeO_2/Ge MIS capacitors fabricated in this work.

4. Summary

We have proposed a novel fabrication technique of SiO_2/Ge MIS structures by low temperature plasma oxidation of ultrathin Si films epitaxially grown on Ge and have successfully fabricated the MIS structures with uniform SiO_2 thickness and flat interfaces, for the first time. It was found that the interface of the fabricated devices is composed of SiO_2/GeO_2/Ge. The oxidation rate of Ge beneath SiO_2 was much slow and, thus, the oxide thickness was almost determined by the thickness of Si films grown epitaxially. The minimum value of N_{ss}, estimated by the Terman method using the C-V data at -50 °C, was in the order of 10^{11} $eV^{-1}cm^{-2}$.

Acknowledgements

This work was partly supported by MIRAI project.

References [1] T. Tezuka et al., EDL-26 (2005) 243 [2] W. P. Bai et al., EDL-26 (2005) 378 [3] A. Dimoulas et al., APL,86 (2005) 223570

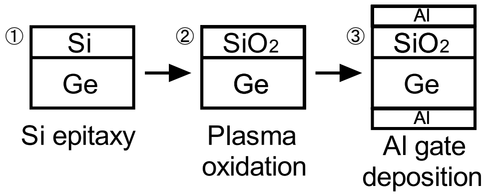

Fig.1 Proposed technique to fabricate SiO_2/Ge MIS capacitors by plasma oxidation of ultrathin Si films on Ge

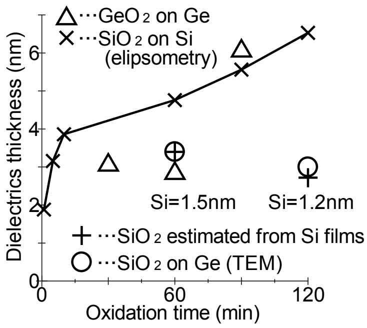

Fig. 2 Comparison of plasma oxidation rate of Si substrates, Ge substrates and Si films on Ge

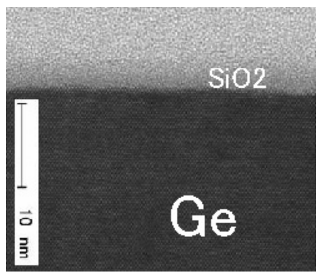

Fig.3 TEM image of SiO_2/GeO_2/Ge MIS capacitor (oxidation time : 60min)

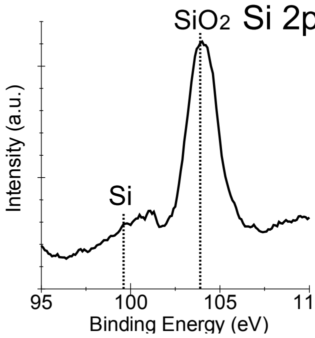

Fig.4 Si 2p spectrum of SiO_2/GeO_2/Ge MIS capacitor (oxidation time : 60min)

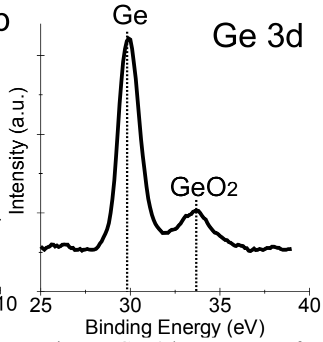

Fig.5 Ge 3d spectrum of SiO_2/GeO_2/Ge MIS capacitor (oxidation time : 60min)

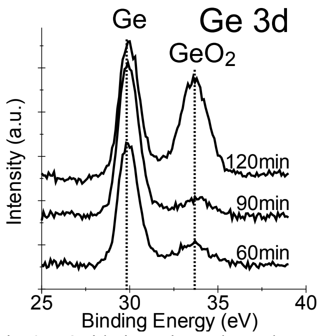

Fig.6 Oxidation time dependence of Ge 3d spectra (oxidation time : 60min)

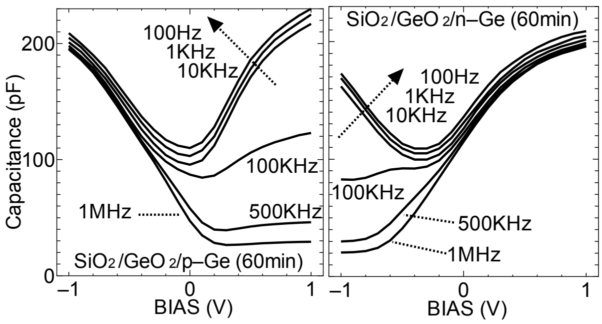

Fig.7 Frequency dispersion of C-V curves of SiO_2/GeO_2/Ge MIS capacitor (oxidation time : 60min)

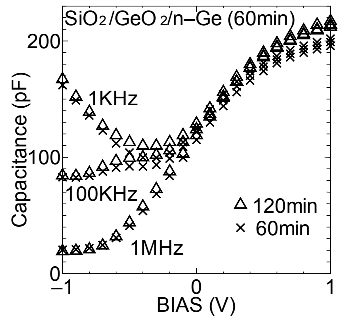

Fig.8 Oxidation time dependence of C-V curves

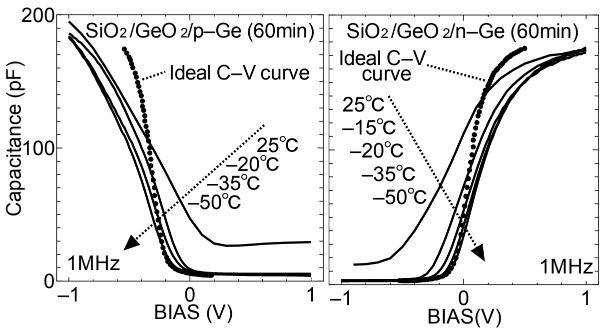

Fig.9 Temperature dependence of C-V curves and calculated ideal C-V curves

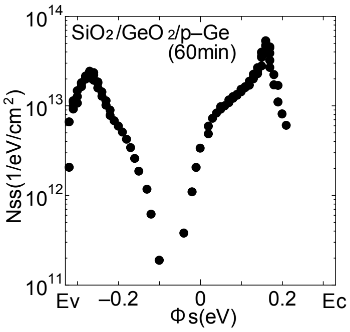

Fig.10 Nss estimated from C-V curve of SiO_2/GeO_2/p-Ge at -50°C

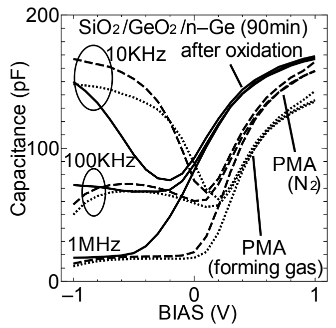

Fig.11 Effects of N_2 anneal and forming gas anneal