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J-6-3

Strong Fermi-level Pinning of Wide Range of Work-function Metals at Valence Band Edge of Germanium

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1. Introduction

Germanium (Ge) devices have been proposed as one of the candidates over the scaling limit of silicon (Si) technology, because Ge has higher mobility in low electric field than Si. In the generation Ge material will be introduced to actual circuits, metal/Ge junctions for ultra-short channel S/D FETs will be required for reducing parasitic resistances. It was reported by using a limited range of work-function metals that Shottky barrier height (SBH) of metal/Ge junction was difficult to change due to the Fermi-level pinning (FLP) at the surface[1]. This paper reports experimental results of metal/Ge junction characteristics, in which a wide range of work function (WF) metals from Y to Pt were studied.

2. Experiment

The RCA cleaning method was employed for Si substrate, but appropriate cleaning process for Ge is still unclear. So, in this work, we used methanol, HCl, H_2O_2+NH_4 and HF cleaning process[2]. The metals were selected from a wide range of WF, as shown in **Fig. 1**. The 50 nm-thick electrode metals were evaporated on the substrates by electron beam in UHV condition (base pressure; 10^{-8}Pa) (except for Au and Al) and thermally in vacuum condition (Au and Al).

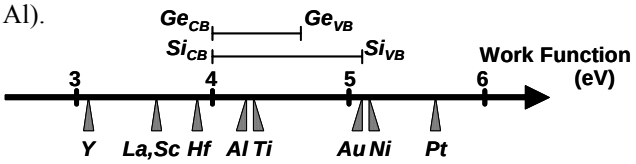

Figure 1 WF of metals[3] that are used in this work. The range of metal WF is enough wide compared with Si and Ge band level.

3. Results

-Metal Work Function Dependence of SBH-

All p-Ge/metal and n-Ge/metal junctions show ohmic and Shottky characteristics, respectively, as shown in **Fig. 2**. On the other hand, in the Si case, shallow WF metals show diode characteristic for p-Si, while ohmic behavior for n-Si. And deep WF metals show the opposite.

SBH was evaluated by the following equations,

$$J = J_s(e^{\frac{qV}{kT}} - 1), \quad J_s = A^* T^2 e^{-\frac{q\phi_b}{kT}}$$

, where J_s is the saturation current density, and A^* is the Richardson constant (about 140 for n-Ge, 260 for n-Si and 80 for p-Si[4]). The J_s was evaluated from a linear extrapolation of current densities at reverse bias condition to V=0. The results for n-Ge were also quantitatively confirmed from $1/C^2$ vs. V plots, as shown in **Fig. 3**. **Fig. 4** shows that SBH values on Si are in a good agreement with the reported values[4], while SBH on Ge very slightly depends on the vacuum WF. This indicates that the Fermi-level of any metals on Ge is close to the valence band edge of Ge.

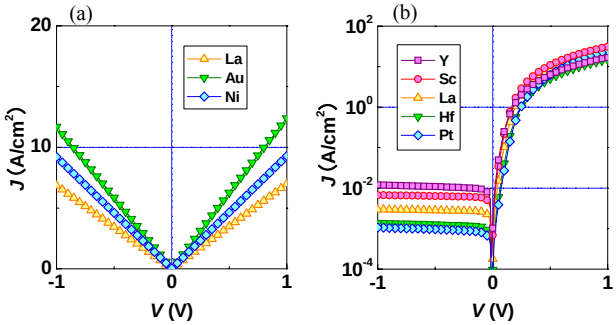

Figure 2 (a) *J-V* characteristics of metal/p-Ge systems. Vertical current axis is linear scale. (b) *J-V* characteristics of metal/n-Ge systems. Vertical current axis is logarithmic scale.

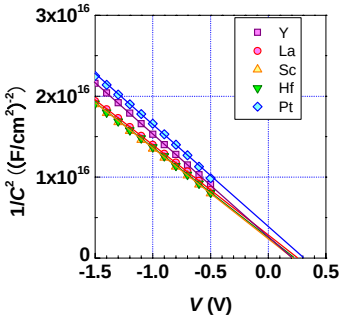

Figure 3 $1/C^2$ vs. V plots for typical metals/n-Ge. SBH values extracted from these plots have good agreement with those extracted from *J-V* plots.

In general, SBH with metal/n-semiconductor junction is expressed as follows.

$$\phi_{bn} = S(\phi_{metal} - \phi_{CNL}) + \phi_{CNL} - \chi_{SC}$$

S parameter defined by $\partial\phi_{bn}/\partial\phi_{metal}$, describes a pinning strength. The S parameter and the charge neutrality level (CNL, ϕ_{CNL}) for Si and Ge are obtained to be 0.27, 4.72 eV and 0.02, 4.58eV for Ge, respectively from the results in **Fig. 4**. It clearly indicates that Ge is pinned more strongly than Si.

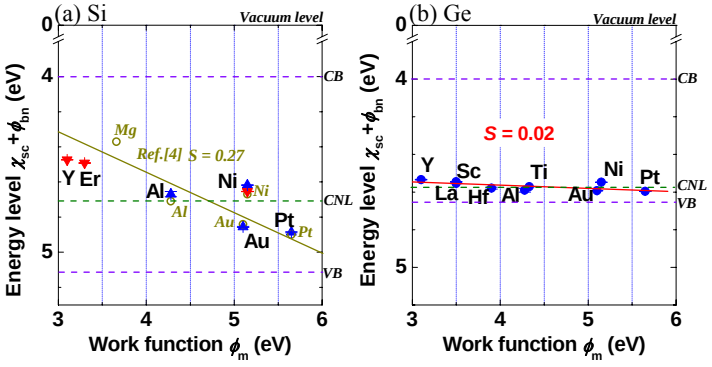

Figure 4 (a) Metal energy level from vacuum level plotted from SBH for metal/p-Si(▼), SBH for metal/n-Si(▲) in this work and reference(○)[4]. (b) Metal energy level from vacuum level plotted from SBH of metal/Ge systems. The S parameter is extracted from the plots by least square method.

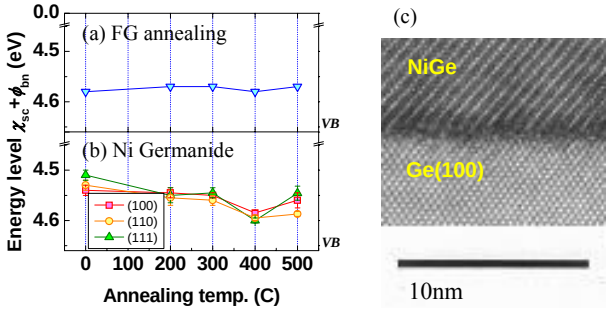

Figure 5 (a) Al energy level at Al/n-Ge interface after various temperatures FG annealing (He+5%H_2). Annealing was performed for 30min. (b) Annealing temperature dependence of Ni(NiGe) energy level for each oriented substrate. (c) Cross sectional TEM image at NiGe/Ge(100) interface annealed at 400°C.

-Forming gas annealing, Germanide, Surface Orientation and Oxidation-

Four kinds of possible SBH modulation techniques were employed; (i) Forming gas (FG) annealing, (ii) germanide reaction, (iii) Ge surface orientation, and (iv) oxidation.

(i) We changed the annealing temperature in the range of 200-500°C. **Fig. 5(a)** shows that FG annealing is ineffective to weaken the FLP.

(ii, iii) Ni was deposited on Ge in UHV. Thermal annealing for NiGe formation was performed in UHV in the range of 200-500 °C for 5min. XRD measurements indicated that all samples were NiGe. SBH values of NiGe/n-Ge are independent of annealing temperature even on different surface orientation (**Fig. 5(b)**). As shown in TEM image (**Fig. 5(c)**), neither interface layer nor roughness is observed.

(iv) We introduced an intentional poor interface. GeO_x was fabricated on cleaned n-Ge substrates by UV ozone treatment for 5 and 60 min at room temperature. The thickness of GeO_x was evaluated as 2.4 and 2.9nm. The result is that SBH value for n-Ge with Y, Au or Al electrode is almost the same as that of non-oxidation samples.

4. Discussion

It was theoretically reported that hydrogen level in Ge is under the valence band[5], then H passivation might be intrinsically invalid for weakening the FLP. However, it is surprising that reacted interface, substrate orientation and oxidation hardly affect SBH values.

Strong FLP indicated existence of enormous interface level. Interface level density (D) in band gap of semiconductor are roughly estimated from the relation proposed by Cowley and Sze[7].

$$D \cong 10^{13} \times \frac{(1-S)}{S}$$

D for Si and Ge are obtained to be roughly ~10^{13} and ~10^{14} /cm^2/eV, respectively. If the FLP of Ge is caused by induced defects, the above modulation techniques should weaken the pinning or move the pinning position. But, since all passivation techniques we tried could not decrease D, it is likely that the strong pinning comes from material inherent properties.

Metal-induced gap states (MIGS) are known as an intrinsic property at metal/semiconductor interface. This is qualitatively understandable from the relation, proposed by Mönch[6].

Table 1 S parameter derived from experiment and calculation for Si and Ge. ε_i of Si is used for $S_{calc.}$ of Ge

	$S_{exp.}$	$S_{calc.}$
Si	0.27	0.10
Ge	0.02	(0.07)

$$S = \frac{0.86}{1+0.29(\varepsilon_\infty - 1)^2 / \varepsilon_i}$$

Calculated and experimental S parameters are summarized in **Table 1**. ε_i is the relative dielectric constant in the effective interfacial dipole region, which is approximately evaluated from the Tomas-Fermi screening length for metal and decay length of MIGS for semiconductor[6]. This estimation is quite reasonable for the strong FLP of Ge.

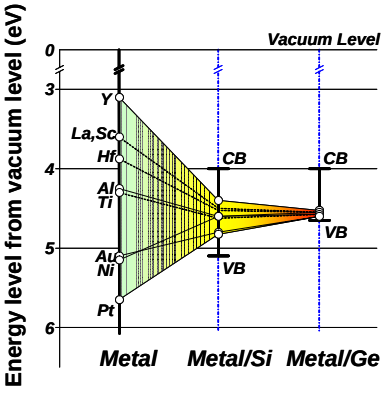

Figure 6 Schematic diagrams of WF and pinning energy level from vacuum level. Energy range becomes narrow in the order of simple metal, metal/Si and metal/Ge.

In **Fig. 6**, the vacuum metal WF and the pinning position at semiconductor surface are summarized in the same energy scale. It is clearly noticed that the controllable energy range in metal/semiconductor system drastically decreases from the vacuum to semiconductors. And it is related to the energy band gap of semiconductor. The CNL which is defined at the interface or surface is very close to the branch point which is defined in bulk semiconductor[8]. This implies that the pinning position is originated from intrinsic semiconductor characteristics rather than from interface reaction in these systems. Thus, it is inferred that the strong FLP and the CNL observed in the experiment on Ge may be caused by the strong MIGS and the branch point inherent to Ge.

5. Conclusion

The strong FLP close to the valence band edge of Ge was observed at the metal/Ge junction. The strong pinning and the pinning level have not been modulated by the several surface treatments. We propose that the strong FLP of Ge is dominantly caused by the MIGS due to the narrow energy band gap of Ge and the CNL is determined by the branch point of Ge.

Reference

[1] E. D. Marshall, et. al.; *MRS Symp. Proc.*, **47**, 161 (1985). [2] K. Kita *et. al.*; *Ext. Abs. SSDM pp. 292* (2003). [3] H. B. Michaelson; *IBM J. Res. Develop.*, **22**, 72 (1978). [4] S. M. Sze; "*The Physics of Semiconductor Devices*" John Willey & Sons Inc. (1981). [5] C. G. Van de Walle and J. Neugebauer; Nature, **423,** 626 (2003). [6] W. Monch; J. Vac. Sci. Tecnol. B; **17**, 1867 (1999). [7] A. M. Cowley and S. M. Sze; J. Appl. Phys.; **36**, 3212 (1965). [8] J. Tersoff; J. Vac. Sci. Tecnol. B; **4**, 1066 (1986).