

J-7-1

Optimization of Hafnium Zirconate (HfZrO_x) Gate Dielectric for Device Performance and Reliability

R. I. Hegde, D. H. Triyoso, S. Kalpat, S. B. Samavedam, J. K. Schaeffer, E. Luckowski, C. Capasso, D. C. Gilmer, M. Raymond, D. Roan, J. Nguyen, L. La, E. Hebert, X-D. Wang, R. Gregory, R. S. Rai, J. Jiang, T. Y. Luo, and B. E. White Jr.

Freescale Semiconductor, Inc., Austin Silicon Technology Solutions (ASTS), 3501 Ed Bluestein Blvd., MD: K10, Austin, TX78721, USA (Tel: 512-933-7072, Fax: 512-933-6962, Rama.Hegde@Freescale.com)

ABSTRACT

Optimization of ZrO₂ content in HfZrO_x gate dielectric for transistor performance, mobility, reliability, and thermal stability is reported for the first time. Incorporation of ZrO₂ into HfO₂ enhances dielectric constant (K) of resulting HfZrO_x which is associated with structural phase transformation from monoclinic to tetragonal. The tetragonal phase increases K of HfZrO_x to a large value as predicted.

INTRODUCTION

Recently, a novel hafnium zirconate (HfZrO_x) alloy gate dielectric was developed to address the shortcomings of HfO₂ [1]. In this paper a systematic investigation was performed on the dielectric properties of HfZrO_x with Ta_xC_y metal gate as a function of ZrO₂ content. Also, boost in the K value of HfZrO_x dielectric is discussed.

EXPERIMENT

The integration follows a standard CMOS process flow on silicon up to HfZrO_x dielectric deposition. The target 30Å ALD HfZrO_x films with four different levels of ZrO₂ (zero, A, B, and C) were deposited at 300°C on RCA cleaned Si. The precursors used for ALD were HfCl₄, ZrCl₄, and D₂O. The Ta_xC_y was used as NMOS gate [2]. A commercial CMOS process technology [3] with activation anneal at 1000°C/5s/N₂ was used to fabricate metal gate/high-K stack MOSFETs.

RESULTS AND DISCUSSION

(a) Transistor Characteristics

Figure 1 shows well-behaved NMOSFET C-V characteristics of HfZrO_x(B) and HfO₂. Compared to HfO₂, the HfZrO_x(B) has a lower CET_{inv} value. The lower CET_{inv} value is due to higher K of the HfZrO_x(B) compared to HfO₂ as shown in Figure 2. Figure 3 plots gate leakage current density (J_g) as a function of CET_{inv}. As shown, the gate leakage for the HfZrO_x(B) devices is over 4 orders of magnitude lower than that of silicon oxynitride. Compared to HfO₂, slightly higher gate leakage current was observed for the HfZrO_x devices. This is due to smaller band gap and lower conduction band offset for HfZrO_x than that of HfO₂ [1]. The electron mobility evaluation in Figure 4 indicated ~7% increase in peak mobility and ~8% increase in mobility at large inversion (high field) for the HfZrO_x(B) devices compared to HfO₂ control. The hole mobility comparison in Figure 5 showed ~9% increase in peak mobility and ~7% increase in mobility at large inversion charge for HfZrO_x(B) devices. Thus, the HfZrO_x dielectric is attractive candidate for CET_{inv} scaling for high performance and low leakage for low standby power applications. The composition optimization of HfZrO_x was performed on long channel transistors fabricated using a shorter flow. Figure 6 shows Hf SIMS depth profiling from the long channel MOSFETs indicating expected levels of ZrO₂ in the HfZrO_x dielectrics. The Table 1 summarizes CET_{inv}, V_t and SS values for the HfZrO_x devices with different levels of ZrO₂. Compared to HfO₂, consistently lower CET_{inv} values were obtained

for HfZrO_x with composition A, B, and C. The K value of HfZrO_x is dependent on HfZrO_x composition as shown in Figure 7 and on HfZrO_x structure as discussed below. In Figure 8, the I_d-V_g characteristics showed that all HfZrO_x devices including HfO₂ have low SS values of 67-68mV/dec, indicating formation of high quality dielectric/Si interfaces. The cross-sectional TEM micrographs in Figure 9 showed that the HfZrO_x dielectrics are polycrystalline with similar bulk dielectric thickness (26-30Å) and interfacial oxide thickness (~9Å). No interaction between the HfZrO_x dielectrics and Si channel was observed after the 1000°C activation anneals. Thus, these HfZrO_x dielectrics showed good thermal stability with Si. The normalized transconductance (G_m) characteristics in Figure 10 confirmed higher G_m for the HfZrO_x devices compared to HfO₂. The BTI characteristics (PBTI and NBTI) for HfZrO_x devices in Figures 11 and 12 showed substantial improvement with ZrO₂ content for NMOS(PMOS) at 1.5V(-2V) stress voltage, respectively. The device performance and reliability improvement is primarily attributed to tetragonal structure of HfZrO_x (see below) with a lower bulk trap density [1].

(b) Boost in Dielectric Constant (K)

The K enhancement for HfZrO_x in Figure 2 and 7 comes from structural phase transformation. Figure 13 shows plan view TEM and selected area electron diffraction (SAD) for 40Å HfO₂ and HfZrO_x(B) dielectric films after Ta_xC_y gate removal. The TEM data showed smaller and more uniform grains for HfZrO_x(B) compared to HfO₂, consistent with AFM images in Figure 14. The SAD data showed tetragonal grains in HfZrO_x(B) dielectric compared to purely monoclinic in HfO₂. Further, thin film XRD results in Figure 15 suggested presence of mainly tetragonal phase for the 40Å HfZrO_x(B) dielectric. The tetragonal ZrO₂ phase is theoretically predicted [4-6] to have higher dielectric constant (K~47) than monoclinic phase (K~20). The improved device characteristics are due to fine grained micro-structure of HfZrO_x with increased grain boundary area that results in less oxygen vacancy. More oxygen in grain boundary will reduce equilibrium concentration of oxygen vacancy in the bulk of the grains.

CONCLUSIONS

Addition of ZrO₂ stabilizes the tetragonal phase and enhances the K value in HfZrO_x devices. The ZrO₂ content needs to be optimized for performance. The HfZrO_x dielectric is an attractive candidate for advanced gate stack applications.

ACKNOWLEDGEMENT

The authors would like to thank Suresh Venkatesan, Director of ASTS, for management support.

REFERENCES

- [1] R. I. Hegde, et al, IEDM, p.39 (2005)
- [2] J. K. Schaeffer, et al, IEDM p.287 (2004)
- [3] A. Perera, et al, IEDM, p.571 (2000)
- [4] H. Kim, et al, J. Mater. Res. **20**, 3125 (2005)
- [5] S. Sayan, et al, App. Phys. Letters **86**, 152902 (2005)
- [6] X. Zhao, et al, Phys. Rev. B **65**, 075105 (2002)

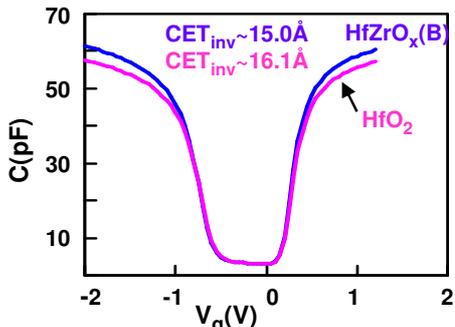


Fig. 1 NMOSFET C-V for HfZrO_x and HfO₂ (W/L=10μmX10μm)

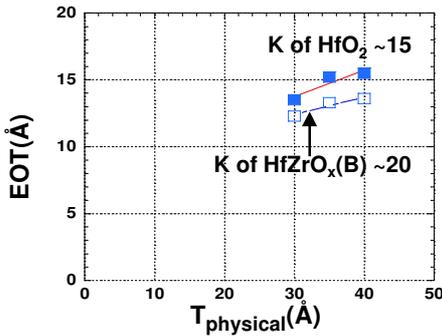


Fig. 2 Dielectric constant of HfZrO_x from EOT vs. physical thickness

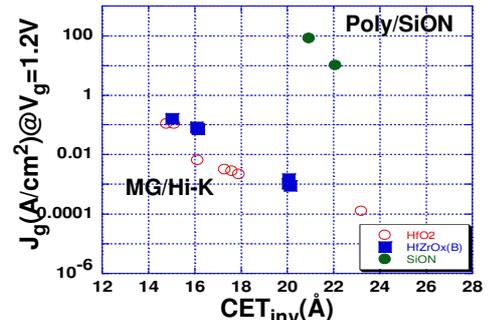


Fig. 3 Gate leakage current density as a function of CET_{inv}

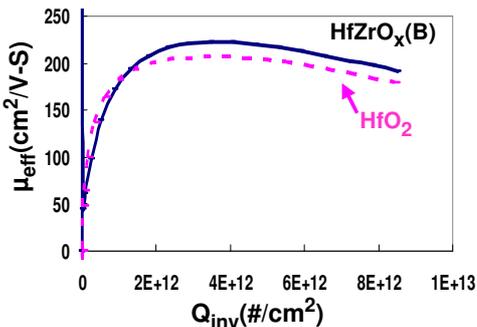


Fig. 4 Electron mobility for HfO₂ and HfZrO_x devices (W/L=10μmX10μm)

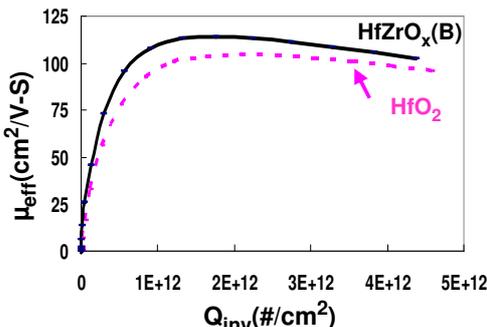


Fig. 5 Hole mobility for HfO₂ and HfZrO_x devices (W/L=10μmX10μm)

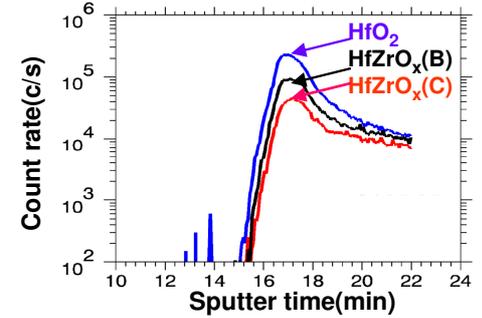


Fig. 6 Hf SIMS depth profiling from HfZrO_x MOSFETs

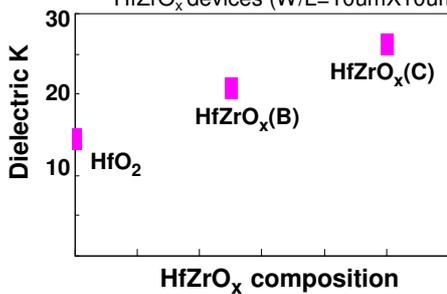


Fig. 7 K value vs. HfZrO_x composition

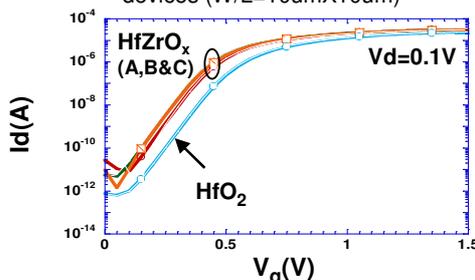


Fig. 8 Id-Vg characteristics of HfZrO_x NMOSFET (W/L=10μmX10μm)

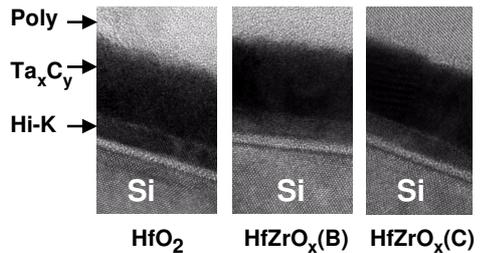


Fig. 9 XTEM images of HfZrO_x NMOSFETs showing good thermal stability with Si

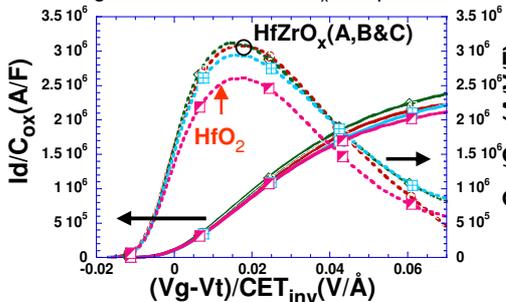


Fig. 10 Normalized G_m characteristics for HfZrO_x devices (W/L=10μmX10μm)

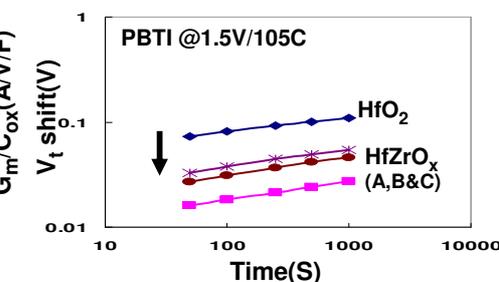


Fig. 11 V_t instability with electrical stress for HfZrO_x NMOSFET (W/L=10μmX10μm)

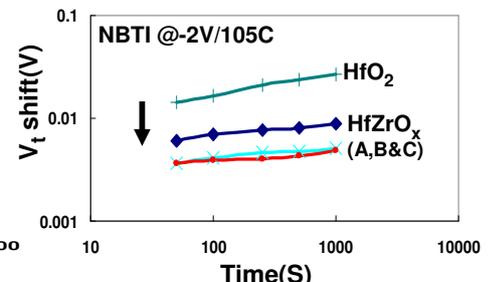


Fig. 12 V_t instability with electrical stress for HfZrO_x PMOSFET (W/L=10μmX10μm)

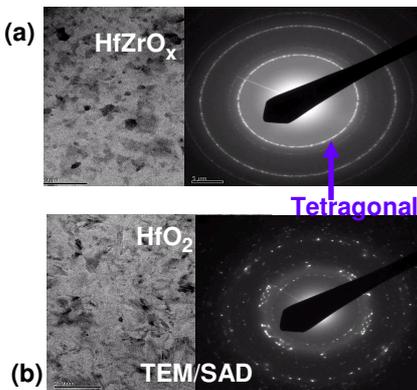


Fig. 13 plan view TEM and SAD of (a) HfZrO_x and (b) HfO₂ films

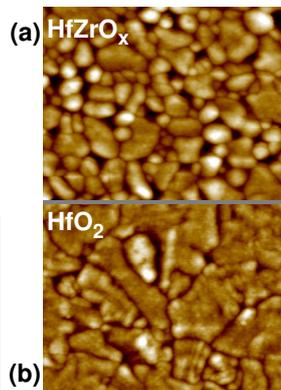


Fig. 14 AFM images of (a) HfZrO_x and (b) HfO₂ films

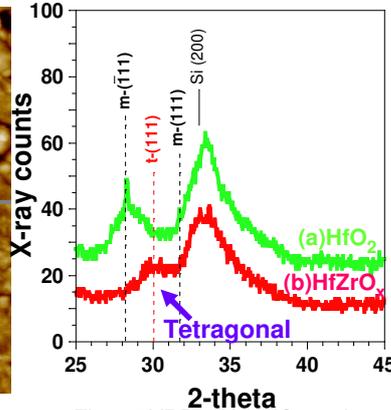


Fig. 15 XRD of (a) HfO₂ and (b) HfZrO_x films

Table I
HfZrO_x NMOSFET results*

	High-K CET _{inv} (Å)	V _t (V)	SS(mV/dec)
HfZrO _x (A)	15.7	0.39	66
HfZrO _x (B)	15.6	0.37	67
HfZrO _x (C)	15.1	0.38	67
HfO ₂	17.5	0.44	68

(*long channel devices using shorter flow)