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Current Transportation Mechanism and Interface States Characterization of Sputtered Gd_2O_3 Gate Dielectrics for ULSI Application

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1. Introduction

High-k gate dielectrics are considered to be the most promising candidates to meet the future ULSI application [1]. Of all the researched high-k materials, Gd_2O_3 thin films have become much more attractive due to its high dielectric constant and excellent thermal stability [2-3]. However, the current transportation mechanism and charge trapping characteristics of sputtered Gd_2O_3 gate dielectrics are still not well developed. In this paper, we investigate the tunneling mechanism of Gd_2O_3 thin films based on gate leakage current measured at elevated temperature. The interface states are characterized in both NMOS and PMOS with Gd_2O_3 gate dielectrics and effectively reduced with increasing the PDA temperature. In addition, the silicon surface band bending characteristics are also proposed to identify the Gd_2O_3/Si interface.

2. Experiments

After standard RCA cleaning, the Gd_2O_3 thin films were deposited by RF sputter at 150W. Some samples were treated with RTA from 500 to 900°C for 30s. Finally, Al was evaporated as the gate and backside contact material. The key process flow of Al/Gd_2O_3/Si MISCAP was shown in Fig.1. Besides, the electrical properties were analyzed by HP4284A for high frequency (100kHz) C-V characterization, and HP4156C for I-V and quasi-static C-V measurements. Al/Gd_2O_3/Si structures of as-deposited and 900°C annealed samples were investigated by TEM images (Fig. 2) and the increase of the interfacial layer was observed due to the change of film composition after PDA treatment [4].

3. Results and discussion

A. Current transportation mechanism of Gd_2O_3

The temperature dependence of the gate leakage current was studied to realize the current transport mechanism. Figure 3 shows the gate leakage currents measured from 303 to 363K of the as-deposited and 600°C PDA samples. As we can see, the experimental results well fit the (Frenkel-Poole) F–P mechanism as shown in the inset of Fig. 3. Figure 4 presents the Arrhenius plots for the currents at several electric fields. The thermally activated behavior further supports that the carrier transportation in Gd_2O_3 is F-P emission. The effective barrier heights, Φ_B, derived from the as-deposited and 600°C annealed samples were 0.97 and 1.62 eV, respectively (Fig. 5). This implies that the PDA treatment effectively eliminates some shallow traps in Gd_2O_3 thin films. Besides, the effective F-P barrier heights of all samples are listed in the inset table of Fig. 5.

B. Interface states characterization of Gd_2O_3

Figure 6 demonstrates the normalized high frequency C-V characteristics and the interface states distribution of NMOS and PMOS with Gd_2O_3 as gate dielectrics. The improved C-V distortion with higher PDA temperature annealing indicates that some acceptor-like interface states were eliminated [5] Figure 7 shows the quasi-static (QCs) and high frequency C–V characteristics of NMOS and PMOS samples with 900°C PDA. The small capacitance offset between high frequency and quasi-static CV and almost the same inversion and accumulation capacitances were obtained. From ref. [6], the integration for the equation

$$\Psi_S(V_1) - \Psi_S(V_2) = \int_{V_1}^{V_2} \left[1 - \frac{C(V_a)}{C_{OX}} \right] dV_a \qquad (1)$$

over the quasi-static capacitance can reveal actual operation of the Al/Gd_2O_3/Si structure as illustrated in Fig. 8. In addition, the interface states density D_{it} as a function of band gap energy by using the QCs/high frequency technique [7] was displayed in inset of Fig. 9. The interface states density of Gd_2O_3 gate dielectrics at mid-gap was observed and found to decrease with increasing PDA temperature due to elimination for defect vacancy of Gd_2O_3 thin film (Fig. 9).

4. Conclusion

For the first time, the current transportation mechanism and interface states characterization of Gd_2O_3 gate dielectrics were demonstrated. The effective barrier heights of Al/Gd_2O_3/Si MISCAP were extracted from well F-P fitting and lower interface states density was obtained in annealed Gd_2O_3 thin films. These Gd_2O_3 gate dielectrics are promising candidates for future ULSI application.

Reference

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n- p- Si sub. **preparation**

RCA clean

***Gd_2O_3* dep. (5 nm)**

With or W/O PDA (N_2 annealing)

Al electrode

Fig.1. The key process flow of Al/Gd_2O_3/Si MISCAP in this work

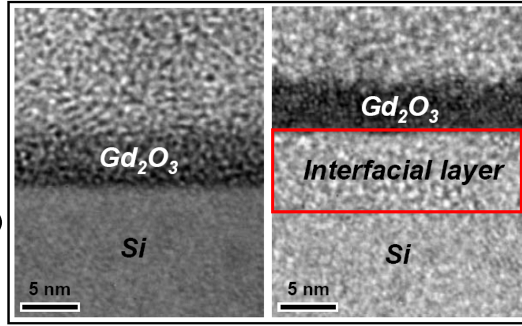
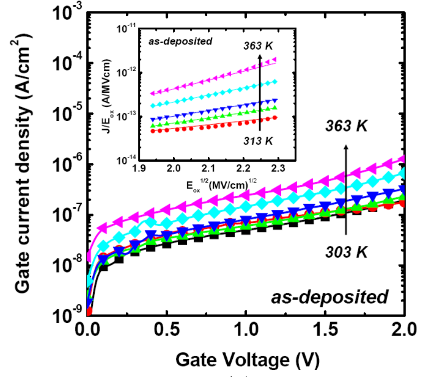
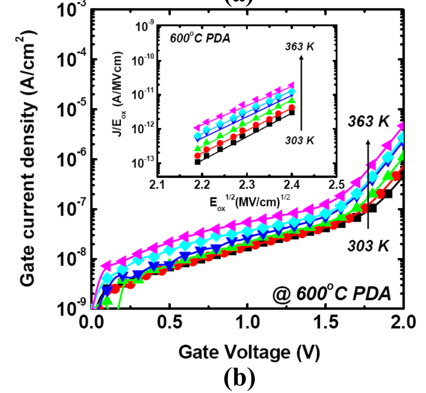


Fig.2. The TEM image of the Gd_2O_3 film (a) without and (b) with 900°C PDA, respectively.





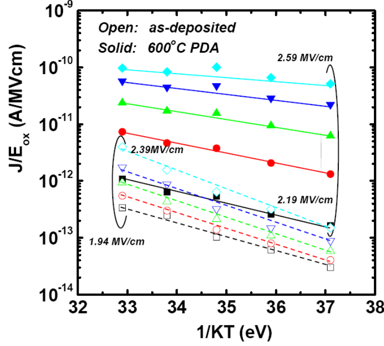


Fig.4. The Arrhenius plots of gate leakage current density under different electrical fields for the Gd_2O_3 gate dielectrics without and with 600°C PDA.

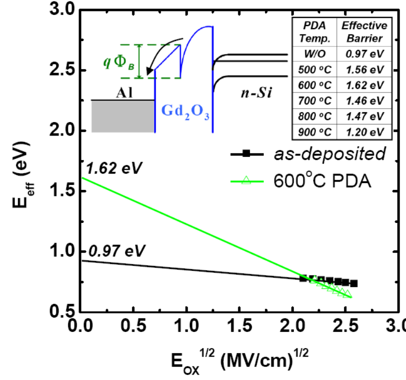
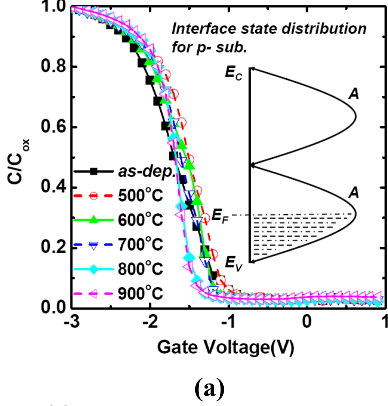


Fig.5. Graphical extrapolation of the F-P barrier height from the dependence of effective activation energy, on the square root of the electric field. Inset table shows F-P barrier height of all samples.

Fig.3. Temperature dependence of gate current density under sub. injection for (a) se-dposited and (b) 600°C PDA Gd_2O_3 gate dielectrics. The inset figure is F-P tunneling fitting.



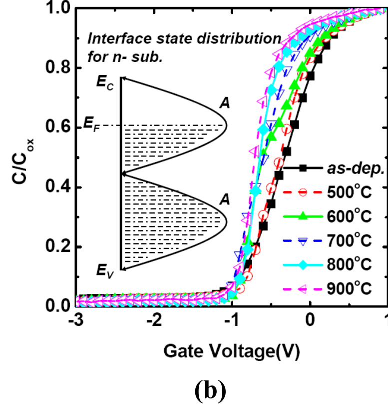
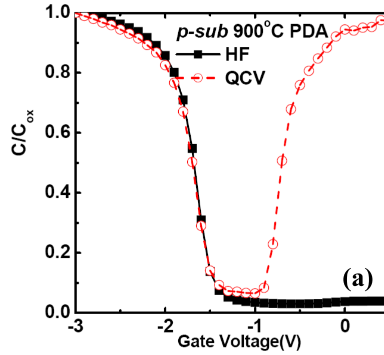


Fig.6. Normalized high-frequency C-V Curve and interface state distribution for (a) NMOS and (b) PMOS Gd_2O_3 gate dielectrics



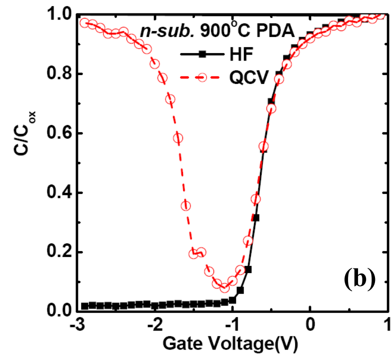


Fig.7. The normalized high-frequency and quasi-static C-V Curve for (a) NMOS and (b) PMOS Gd_2O_3 gate dielectrics with 900°C PDA.

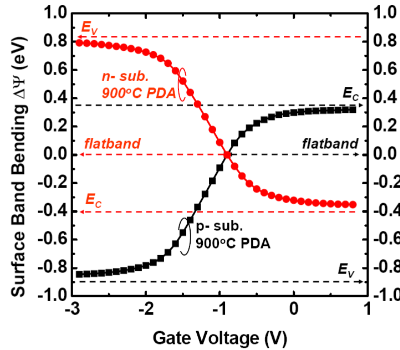


Fig.8. Surface band bending Ψs inferred from the measured quasi-static C-V using Berglund's method (Ref. 6).

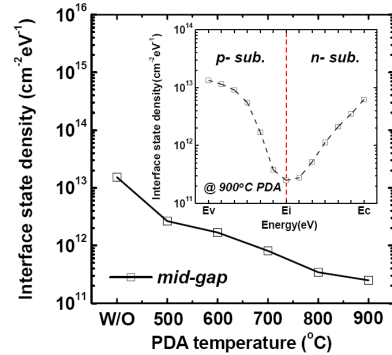


Fig.9. Interface-state density of Gd_2O_3 gate dielectrics with different PDA temperature for mid-gap plotted.