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Highly scalable and WF-tunable Ni(Pt)Si / SiON TOSI-gate CMOS devices obtained in a CMP-less integration scheme

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Abstract
In this paper, we assess the threshold voltage adjustment window of TOtally SIlicided (TOSI) gate CMOS devices obtained in a CMP-less integration flow via the incorporation of dopants into the Ni(Pt)Si gate electrode. A detailed analysis of device and gate stack characteristics allows us to define the most suitable TOSI-gate solution for the CMP-less integration scheme targeting future Low Power applications.

1. Introduction

TOSI gates are considered as a smart and low-cost solution to obtain metal gates in CMOS devices for both their integration easiness and the possibility of work function (WF) tuning by ion implantion prior to the gate silicidation as proven for NiSi on SiO_2 [1-4]. Recently, it has been shown that TOSI-gates can be obtained in a close-to-standard CMOS flow without any additional CMP-process by simultaneously siliciding the ultra-low gate and the epitaxially raised active areas [5]. The industrial viability of this approach has been demonstrated by the successful fabrication of SRAM cells containing midgap-NiSi gate electrodes [6]. In this paper, we focus on the threshold voltage tuning window by ion incorporation into the TOSI-gate taking into account the specific constraints of the CMP-less approach. In particular, the common silicidation of gate and junctions requires the limitation of the thermal budget of the TOSI-process and the use of monosilicides such as NiSi or $Ni_{1-x}Pt_xSi$ - the latter having shown interesting properties for total gate and junction silicidation [7, 8] – in order to obtain scalable junctions.

2. TOSI-gate integration

The CMP-less TOSI-gate integration is schematically shown in Fig. 1. On the 17Å-EOT DPN nitrided SiO_2, a layer of 30nm poly-Si is deposited. Next, gate predoping with B, BF_2, P (all $3x10^{15}cm^{-2}$) or As ($2x10^{15}cm^{-2}$) is carried out and the poly-Si is capped by a 70nm-thick oxide hard mask. After patterning and LDD implantation, a selective epitaxy step is inserted to raise the active areas before the S/D implantations. After annealing, the hard mask is removed and the total gate electrode and the upper part of the junctions are silicided with 20nm Ni or NiPt(5%)Si using a two step anneal (RTP1: 290°C 240s, RTP2: 450°C 90s). For P- and B-predoping a split with reduced thermal budget (RTB) has been added (RTP1: 290°C 120s, RTP2: 450°C 60s). For better comparison, poly-Si- and undoped TOSI-gate references have been added. Fig. 2 shows a TEM picture of a 30nm-(P)-NiSi-TOSI device. Fig. 3 demonstrates the full gate silicidation for NiSi and NiPtSi on SiON gate stacks.

3. Threshold Voltage and Gate stack analysis

Figure 4 shows the impact of the gate predoping prior to Ni silicidation on the threshold voltage. For all gate lengths, the previously doped TOSI-gate splits present lower threshold voltage (V_{th}) values than the undoped TOSI-gate splits corresponding to a WF shift towards the band edges of up to 300mV. Figure 5 proves that in all cases the absolute V_{th} value is well controlled by the channel doping ruling out possible B cross-diffusion effects during the silicidation process. C-V measurements have been carried out on all NiSi and NiPtSi splits to assess the effective reduction of the CET_{inv}-value after the TOSI process (cf. Fig. 6-9). These values are correlated in Fig. 10 with the V_{th}-extracted WF values to define the optimum process. Related to slow-downs in the silicidation kinetics [9], not all doped splits are totally silicided for the chosen thermal budget. A residual poly-depletion is found for (BF_2)-, (As)-, RTB-(P)-NiSi and all n-like NiPtSi splits. The best WF – CET_{inv} trade-off is found for (P) and (B)-NiSi presenting WFs of 4.4 and 4.85eV and complete poly-depletion suppression. Fig. 11 presents the I_g-V_g characteristics for these splits, proving equivalent leakage behavior with respect to the poly-Si references.

4. Device characteristics

In Fig. 12 we plotted the performance data of the (B)- and (P)-NiSi-TOSI gate transistors featuring minimum gate lengths of 30nm. Fig. 13 and 14 show the I_d-V_g- and I_d-V_d-characteristics of individual N and PMOS transistors. Note that no stress engineering has been applied leaving high margins for performance optimisation. Equally promising is the transfer of the modulated NiSi-TOSI-gate stack on FDSOI as proven in Fig. 15: for equivalent I_{on}-value, we find a significant reduction of I_{off} thanks to better *DIBL* and *SS* control.

5. Conclusion

In this work, we have demonstrated the feasibility of threshold voltage adjustment in NiSi-based TOSI-gate devices obtained in a CMP-less via gate predoping. Best WF modulation for full poly-depletion suppression has been demonstrated for (B)- and (P)-NiSi-TOSI gate stacks with WF values of 4.85 and 4.4eV respectively. NiPt(5%)Si is suitable for p-like electrodes, but full gate silicidation after n-type implantation requires higher thermal budgets. The WF tuning is scalable down to 30nm gate length, which makes this module very promising for implementation on bulk or SOI for Low Power applications.

Acknowledgements
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References

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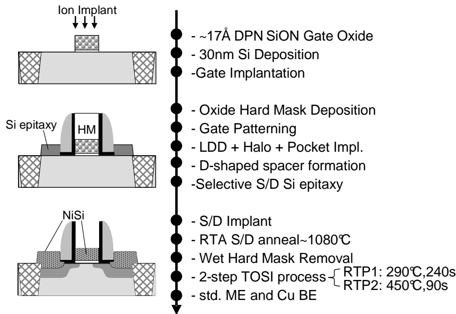

Fig. 1: Scheme of the CMP-less CMOS integration flow.

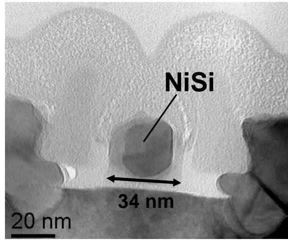

Fig. 2: TEM picture of a 30nm–(P)-NiSi-TOSI-gate NMOSFET.

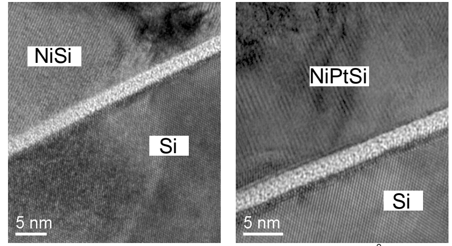

Fig. 3: Zoom on the TOSI-gate on 17Å-EOT SiON: (B)-NiSi (left) and (BF_2)- NiPtSi (right).

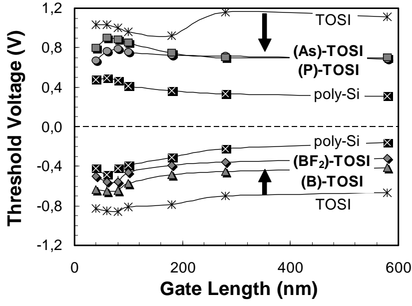

Fig. 4: Threshold voltage versus gate length for NiSi-TOSI with and without gate predoping for N and PMOS devices.

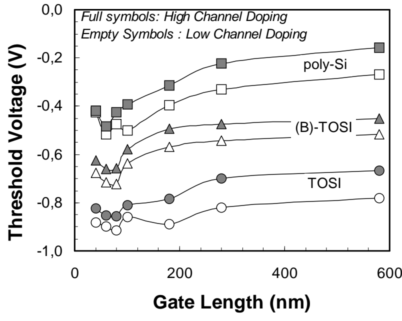

Fig. 5: Impact of channel doping for TOSI-gated and poly-Si gated PMOS transistors excluding B-cross-diffusion effects.

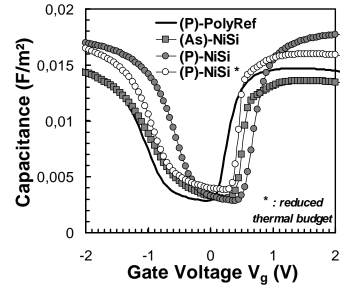

Fig. 6: C-V curves for NiSi-TOSI-gated NMOS devices with different dopants.

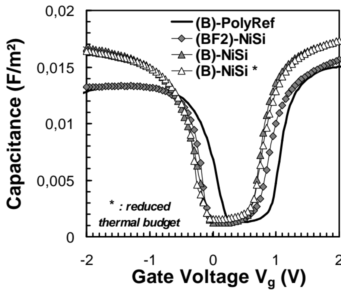

Fig. 7: C-V curves for NiSi-TOSI-gated PMOS devices with different dopants.

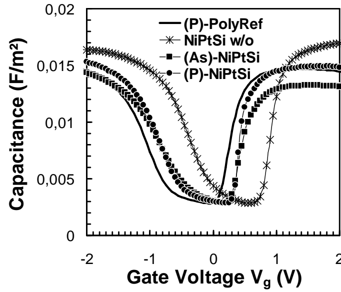

Fig. 8: C-V curves for NiPtSi-TOSI-gated NMOS devices with different dopants.

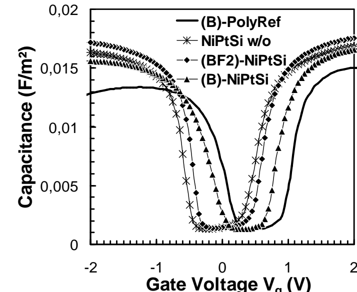

Fig. 9: C-V curves for NiPtSi-TOSI-gated PMOS devices with different dopants.

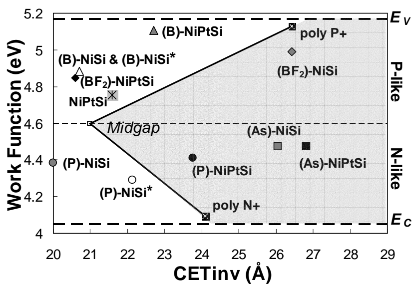

Fig. 10: Summary of the WF versus *CETinv* trade-off for the different TOSI-gate stack approaches.

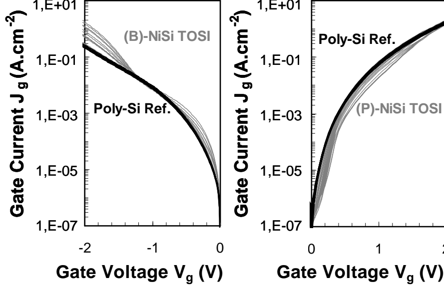

Fig. 11: Gate leakage statistics of (B)- and (P)-NiSi-TOSI devices (S = 100µm²).

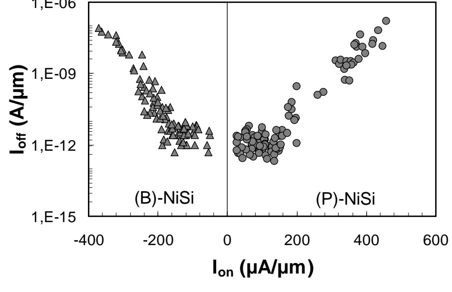

Fig. 12: Performance chart of (B)- and (P)-NiSi TOSI devices.

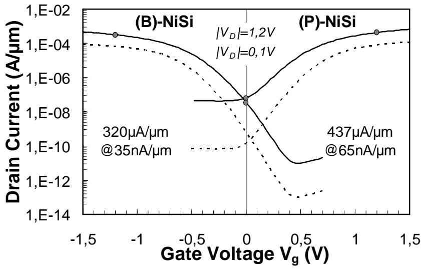

Fig. 13: I_d-V_g characteristics of short (B)- and (P)-NiSi-TOSI-gate devices (L_g = 35nm).

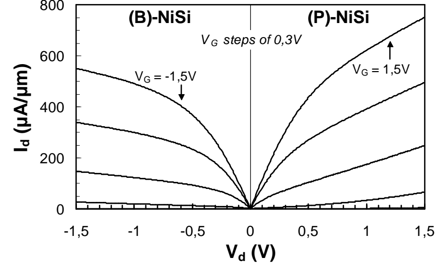

Fig. 14: Output characteristics of short (B)- and (P)-NiSi-TOSI-gate devices (L_g = 35nm).

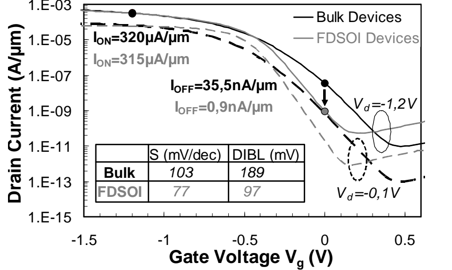

Fig. 15: Comparison of highly scaled (B)-NiSi TOSI-gate devices on bulk and FDSOI.