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Sub-30 nm P-channel Schottky Source/Drain FinFETs: Integration of Pt_3Si FUSI Metal Gate and High-κ Dielectric

Rinus T. P. Lee[1], Kian-Ming Tan[1], Andy Eu-Jin Lim[1], Tsung-Yang Liow[1], Guo-Qiang Lo[3], Ganesh Samudra[1], Dong Zhi Chi[2], and Yee-Chia Yeo[1]

[1]Silicon Nano Device Lab., Dept .of Electrical & Computer Engineering, National University of Singapore, 119260 Singapore.
[2]Institute of Materials Research and Engineering, 3 Research Link, 117260 Singapore.
[3]Institute of Microelectronics, 11 Science Park Road, 117685 Singapore.
Phone: +65 6516-2298, Fax: +65 6779-1103, E-mail: yeo@ieee.org

ABSTRACT

Sub-30 nm Schottky source/drain (S/D) FinFETs with metal and poly-Si gate electrodes were fabricated. A novel self-aligned platinum silicidation process that integrates both a Pt-rich Pt_3Si FUSI metal gate and a PtSi S/D silicide was demonstrated. With the improved silicidation process, 27 nm FUSI Pt_3Si metal gate FinFETs with PtSi S/D were fabricated. Compared with a PtSi S/D FinFET with poly-Si gate, the device with Pt_3Si metal gate gives significantly higher I_{Dsat} due to the elimination of gate depletion effects.

INTRODUCTION

FinFETs or multiple-gate transistors have superior control of short-channel effects and enable scalability well beyond the 32 nm technology node. On the other hand, Schottky source/drain (S/D) transistors [1,2], which essentially replace the highly-doped S/D junction with a metallic junction, offers low sheet and specific contact resistance and a reduced thermal budget for the integration of metal gates on high-κ dielectrics [3]. The integration of metal gates eliminates gate depletion, and increases the inversion charge density and drive current I_{Dsat} for a given gate overdrive. Therefore it is advantageous to integrate metal gate and Schottky S/D on FinFET devices to realize transistors with ultimate device scalability.

In this work, sub-30 nm PtSi Schottky S/D FinFETs with metal and poly-Si gate electrodes were fabricated. A novel self-aligned silicidation process was employed, forming Pt_3Si gate electrode and PtSi S/D in a single silicidation process. This is the first demonstration of FUSI Pt_3Si metal gate/high-κ dielectric integrated in Schottky S/D FinFETs with PtSi S/D in a single silicidation process.

DEVICE FABRICATION

Fig. 1 summarizes the key process steps employed in the fabrication of the Schottky S/D FinFETs. The two device structures realized in this work are shown in Fig. 2, including (a) poly-Si gate FinFET with PtSi Schottky S/D, and (b) FUSI Pt_3Si metal gate FinFET with PtSi Schottky S/D.

8-inch SOI substrates with 45 nm thick Si film on 140 nm buried oxide were used. Active regions with fin widths down to 30 nm were defined using 248 nm lithography, resist trimming, and reactive ion etching. The doping concentration in the fins is about 10^{16} cm^{-3}. SiO_2 (EOT = 3 nm) and Al_2O_3 (t_{phys} = 5 nm, EOT = 3 nm) were used as the gate dielectrics for poly-Si gate and FUSI gate FinFETs, respectively. Undoped poly-Si was then deposited. For the devices in Fig. 2(a), the poly-Si was subsequently p^+ doped. Gate lithography and gate etch were then performed. Fig. 3 (b) and (c) show the SEM images of the FinFET structures with a 20 nm tall (undoped) and 90 nm (doped) tall poly-Si gates for the FUSI and non-FUSI devices, respectively. SiN/SiO_2 composite slim spacers with a spacer width of less than 10 nm were formed. Pt films with different thicknesses were deposited followed by silicidation to form Pt_3Si and/or PtSi on the gate, source and drain regions. The TEM image of a typical poly-Si gate Schottky S/D FinFET with PtSi S/D is shown in Fig. 3(a). The completed devices were directly probed.

RESULTS AND DISCUSSIONS

A. Material Characterization and Process Development

Simultaneous integration of Pt silicides as FUSI metal gate and Schottky S/D silicide requires extensive material characterization to identify a good process window, achieving self-aligned silicidation in a single silicidation process.

The XRD spectra in Fig. 4 show the formation of PtSi and Pt_3Si for Pt:Si film thickness ratios of 1:1 and 2:1, respectively. This allows one to select the required silicide phase for optimal threshold voltage control, with the Pt-rich phase having a higher work function [4]. It is known that Fermi-level pinning occurs between $PtSi_x$ and a high-κ gate dielectric like HfO_2, and that increasing the Pt content brings the V_{FB} of the $PtSi_x/HfO_2$ stack towards that of $PtSi/SiO_2$ stack [5]. A similar effect was observed here. The *C-V* curves in Fig. 5 show that similar flatband voltages were obtained for $PtSi/SiO_2$ and Pt_3Si/Al_2O_3 gate stacks.

After the silicidation process, the selective removal of unreacted Pt without removing the Pt-rich silicide is a process integration challenge which was solved in this work. Line patterns of PtSi and Pt_3Si were formed during silicidation, and aqua regia (70°C, 60s) was employed to remove any unreacted Pt. Electrical measurements show that PtSi lines survived the wet etch (Fig. 6a), while Pt_3Si lines were removed (Fig. 6b). By introducing an additional O_2 annealing step prior to the aqua regia etch, O_2 diffuses through the grain boundaries of Pt and forms a thin SiO_x passivation layer on the surface of the Pt-rich silicide surface [6]. This layer protects the Pt_3Si film during the removal of unreacted Pt, allowing Pt_3Si patterns to be formed (Fig. 6c). Fig. 7a-d illustrates the novel process which was adopted in device fabrication.

B. Device Characterization.

Fig. 8 and 9 show the device characteristics of poly-Si gate Schottky S/D FinFETs with gate length L_G = 29 nm. Good subthreshold swing of ~ 100 mV/dec. and drain induced barrier lowering of 0.26 V/V were obtained for these devices. Poly-Si gate Schottky S/D FinFET delivers a drive current of ~ 211 μA/μm at $V_{DS} = |V_{GS} - V_T| = 1V$. Fig. 10 summarizes the subthreshold swing and I_{on}/I_{off} ratios for poly-Si gate Schottky S/D FinFETs with nominal L_G ranging from 30 to 50 nm.

Fig. 11a shows the TEM image of a FinFET with L_G = 27 nm, FUSI Pt_3Si metal gate, and PtSi S/D. HRTEM reveals a good FUSI Pt_3Si-Al_2O_3 interface with no evidence of Pt penetration into the gate dielectric (Fig. 11b). The I_{DS}-V_{DS} plot for the FUSI Pt_3Si metal gate Schottky S/D FinFET is shown in Fig. 12, demonstrating good device characterisitics. A drive current of ~291 μA/μm at $V_{DS} = |V_{GS} - V_T| = 1V$ was obtained. Compared to a 29 nm poly-Si gate Schottky S/D FinFET with the same EOT, the I_{Dsat} is ~22 % higher, after adjustment for the slight L_G discrepancy. The higher I_{Dsat} is attributed to the elimination of the gate depletion effects.

CONCLUSION

We reported the first demonstration of PtSi Schottky S/D FinFETs with FUSI Pt_3Si metal gate, Al_2O_3 gate dielectric, and gate lengths down to 27 nm. A novel self-aligned silicidation process was employed to obtain two different phases of platinum silicide for gate electrode and S/D applications. The FUSI Pt_3Si gate contributed significant improvement in drive current performance. A combination of the FinFET structure with metal gate/high-κ dielectric and Schottky S/D technologies could potentially realize CMOS devices with superior scalability and performance.

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- Fin definition
- **Gate stack formation:**
  - 90 nm poly-Si on 3 nm SiO_2 or
  - 20 nm poly-Si (for FUSI) on 5nm Al_2O_3
- **Gate implant: for 90 nm poly-Si gate**
- **Gate activation: for 90 nm poly-Si gate**
- Gate definition
- SiN/SiO_2 slim spacer formation
- **Metal Deposition:**
  - 20 nm Pt for 90 nm poly-Si gate
  - 25 nm Pt for FUSI
- Silicidation
- Selective Pt removal

Fig. 1. Process sequence employed in the fabrication of Schottky S/D FinFETs with poly-Si gates and FUSI Pt_3Si gate.

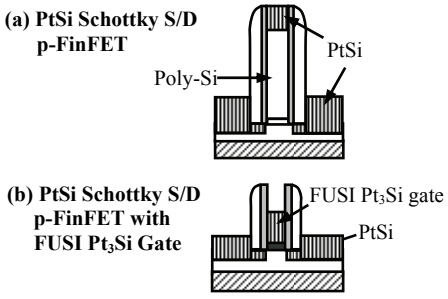

Fig. 2. Schematics showing Schottky S/D FinFETs with (a) poly-Si gate and (b) FUSI Pt_3Si metal gate.

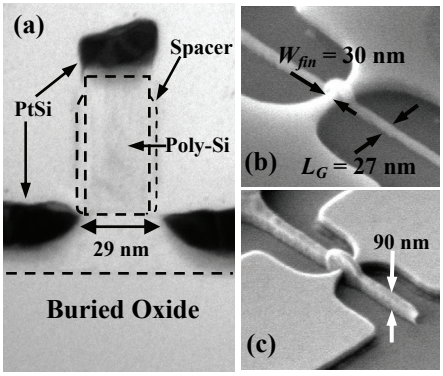

Fig. 3. (a) TEM image showing a transistor with L_G = 29 nm poly-Si gate and PtSi S/D, (b) SEM image of a FinFET before full silicidation of a 20 nm tall poly-Si gate, and (c) SEM image of a FinFET with a 90 nm tall poly-Si gate.

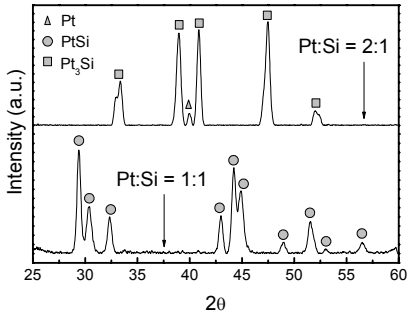

Fig. 4. XRD spectra show the formation of PtSi and Pt_3Si with Pt:Si film thickness ratios of 1:1 and 2:1, respectively. Silicidation was performed on a 20 nm polysilicon/Al_2O_3 gate stack at 400 °C for 60s in N_2 ambient.

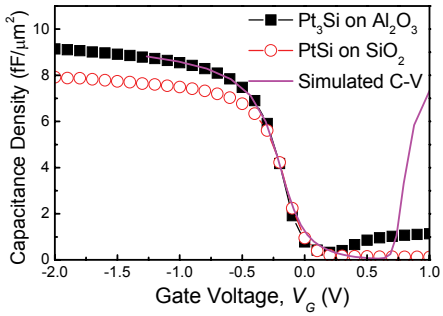

Fig. 5. *C-V* curves of Pt_3Si/Al_2O_3 and $PtSi/SiO_2$ capacitors show similar V_{FB} values. This suggests possibly a relaxation of the Fermi-level pinning on high-κ dielectric.

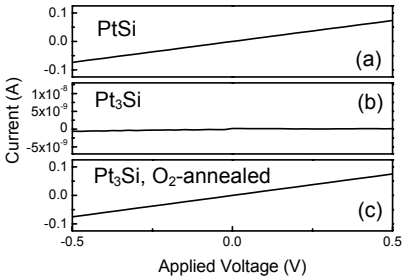

Fig. 6. *I-V* characteristics of line patterns of PtSi and Pt_3Si treated with aqua regia at 70 °C. (a) PtSi, single step anneal in N_2, (b) Pt_3Si single step anneal in N_2, and (c) Pt_3Si formed with a two-step anneal (in N_2 followed by in O_2).

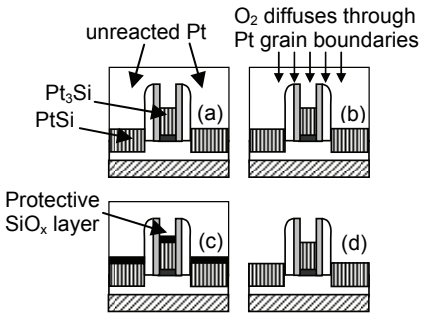

Fig. 7. Schematic showing a novel process flow that forms (a) the Pt_3Si FUSI gate, (b) an O_2-anneal that forms (c) an oxide passivation on Pt_3Si, and (d) the removal of excess Pt metal without removing the Pt-rich Pt_3Si material.

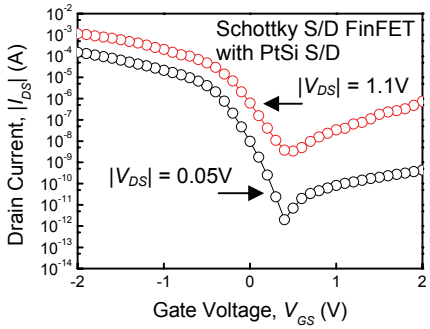

Fig. 8. Typical I_{DS}-V_{GS} characteristics for a PtSi Schottky S/D FinFET with 29 nm L_G and poly-Si gate. The device exhibited good subthreshold swing and drain-induced barrier lowering.

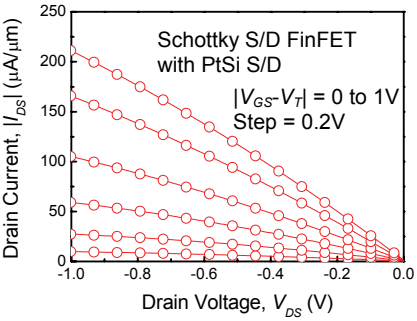

Fig. 9. Typical I_{DS}-V_{DS} characteristic of 29 nm L_G poly-Si gate Schottky S/D FinFETs with PtSi S/D shows I_{DSAT} ~ 211 μA/μm at $|V_{DS}| = |V_{GS} - V_T| = 1V$.

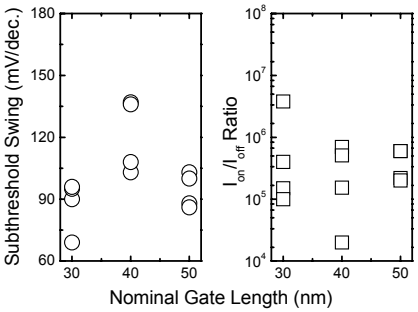

Fig. 10. Subthreshold swing and I_{on}/I_{off} ratio performance of poly-Si gate FinFETs with PtSi Schottky S/D. $I_{on} = I_{DS}@|V_{DS}| = |V_G - V_T| = 1.1$ V, $I_{off} = I_{DS}@V_G = 0$, $|V_{DS}| = 1.1$ V.

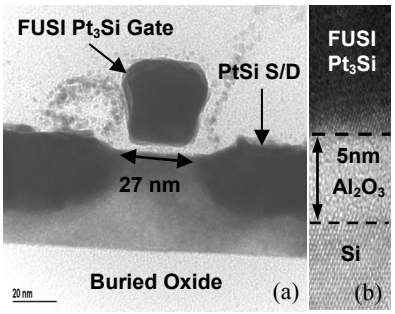

Fig. 11. (a) TEM image of a transistor with a 27 nm FUSI Pt_3Si metal gate on Al_2O_3 with PtSi Schottky S/D, and (b) HRTEM image of the FUSI-Pt_3Si/Al_2O_3 gate stack shows a good Pt_3Si-Al_2O_3 interface.

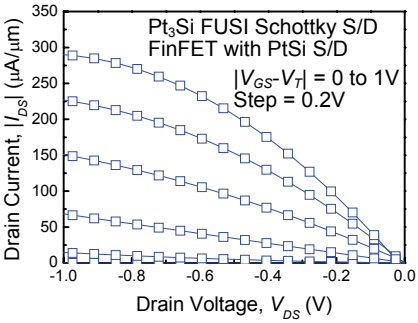

Fig. 12. Typical I_{DS}-V_{DS} characteristic of 27 nm L_G Pt_3Si FUSI gate Schottky S/D FinFETs with PtSi S/D, showing I_{DSAT} ~ 291 μA/μm at $|V_{DS}| = |V_{GS} - V_T| = 1V$.