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Effects of Optimization of Gate Edge Profile on sub-45nm Metal Gate High-k Dielectric Metal-Oxide-Semiconductor Field Effect Transistors Characteristics

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ABSTRACT

The impact of process integration on device characteristics of metal gate/high-k devices was investigated systematically. It was found that the profile of the gate stack edge and subsequent processes should be optimized to achieve low gate-induced drain leakage (GIDL), gate leakage, and high drive current. For low standby power (LSTP) applications, a protruded high-k dielectric layer was more desirable. With an optimized gate edge profile, we achieved 100X lower off-state current compared to previous reported results. However, the degradation in saturation current was minimal.

INTRODUCTION

It is well recognized that high-k dielectrics provide a low off-state leakage current, which is extremely useful for low standby power (LSTP) applications. Intrinsically, high-k devices have decreased gate leakage due to their increased physical thickness for the same equivalent oxide thickness (EOT). Also, it has been reported that high-k devices are better for controlling gate-induced drain leakage (GIDL) and reducing I_{gate} than thin SiON devices [1-4].

In integrating conventional SiON with poly-Si gate stack devices, gate re-oxidation is performed to anneal out process-induced defects (PIDs) and to round the gate bottom edge profile to reduce the vertical field [5-6]. This rounded edge suppresses GIDL and improves hot carrier reliability. When integrating a high-k/metal gate stack, however, this gate re-oxidation process is difficult because of the metal electrode oxidation. In addition, it is expected that high-k dielectric yields a higher vertical field due to its higher dielectric constant, which in turn increases GIDL. Therefore, a high-k undercut followed by an oxide gap fill or nitride layer may suppress GIDL. However, the effect of this gate stack structure on off-state leakage current has not yet been systematically studied.

EXPERIMENTAL

Various thickness combinations of top hafnium oxide (HfO_2) and bottom silicon dioxide (SiO_2) were prepared using <70 nm TiN gate metal-oxide semiconductor field-effect transistor (MOSFET) fabrication process (Fig. 1). In this flow, HfO_2 films (3 - 5nm) were atomic layer deposited (ALD) on top of a 0.6nm ~1.9nm bottom SiO_2 layer. After gate patterning, the gate dielectric layer in the source/drain (S/D) extension region was removed with a wet or dry etch. The wet and dry etching and cleaning methods were optimized to minimize dielectric damage and to control the gate edge profile (Fig. 2). Then, a thin nitride layer was deposited to protect the gate dielectric films. Lightly doped drain (LDD) and halo were implanted through this thin nitride layer, with an optimized implantation dose and energy process to ensure a proper overlap of LDD and control of short channel behaviors and GIDL. S/D activation and post-metallization annealing were then performed. Equivalent oxide thickness (EOT) ranged from 0.9nm to 2.8nm after device fabrication. For comparison, 2.5nm SiON with a poly-Si device and HfO_2 with a TiSiN gate device were also fabricated. L_{gate} was in 60~80 nm range.

Fig. 3 shows typical GIDL characteristics for the thin SiON and HfO_2 (EOT=1.2 nm) devices. For the thin SiON transistor, the dramatic increase of I_g led to increased drain-to-gate leakage current. Compared to the SiON device, the high-k device achieved an excellent I_{off} (GIDL) as well as reduced I_g.

RESULTS AND DISCUSSION

Fig. 4 shows how the gate edge profile affects GIDL. A dramatic decrease in GIDL and I_g was observed for the more protruded high-k dielectric structure even though linear and saturation current voltage (I-V) characteristics of both devices are almost identical. According to a MEDICI simulation, a laterally recessed or protruded high-k edge structure is more desirable for suppressing GIDL due to the reduced vertical field caused by nitride (i.e., thicker EOT) and the reduced doping concentration caused by the increased LDD implantation buffer layer resulting in reduced gate overlap area, respectively (Fig. 5). However, the experimental results indicate that leakage current increased dramatically as the lateral high-k recess was increased. This discrepancy between the simulation and experimental results is mainly due to the leakage path formation in the heterogeneous interface between the high-k and nitride. Since the maximum vertical electric field ($E_{m,max}$) is located in the gate overlap region, GIDL increases for intermediately recessed (0~5 nm) structures (Fig. 6).

To clean and etch out the residual metal gate and high-k layer after poly-Si/metal gate stack patterning, wet etch and dry etch techniques were developed. Transmission electron microscopy (TEM) images show that the profiles at the gate edge after gate etch were almost identical for both wet and dry etch (Fig. 7). However, the gate-to-substrate leakage current and the gate-to-drain leakage current increased in the plasma-treated devices, indicating that plasma damage could increase off-state leakage. Using our novel wet etch technique, gate leakage currents were dramatically reduced while other device parameters were almost identical.

Dielectric breakdown characteristics are shown in Fig. 8. Inversion Voltage breakdown (V_{BD}) in the recessed high-k structure decreased. The wider distribution of I_{gate} was due to the leakage path formation in the heterogeneous interface between the high-k and nitride in the gate edge recessed structure (Fig. 9). ΔI_{dlin} under drain avalanche hot carrier (DAHC) and bias instability (BI) stresses is shown in Fig. 10-(a). Under DAHC stress, I_d difference between the recessed and the protruded structures was insignificant. The reason was that both devices showed almost identical I_{sub}/I_b at DAHC condition, which resulted in the similar degradation behavior (Fig. 10-(b)). In the case of BI stress, the increased I_g in the recessed devices led to higher ΔI_{dlin}. Furthermore, this degradation did not fully recovered during relaxation stages (V_g=-1.0V), indicating permanent damage was generated. However, the protruded device fully recovered during the relaxation stage, indicating charge trapping and detrapping is the main factor. From our previous experiments, it is expected that the interface degradation would be negligible [7].

In protruded structure, I_{on} can be degraded due to the increased R_{ext}, which is induced by blocking LDD and halo implantation. For the protruded structures, however, the decrease of I_{on} was about 5% (Fig. 11). After careful process and device optimization, 100X lower off-state leakage current with reasonable I_{on} was achieved comparing to previously reported values (Fig. 12).

CONCLUSION

The impacts of process integration on device characteristics of metal gate/high-k device were investigated systematically. Excellent GIDL controllability was achieved by optimizing the gate edge profile and process. After careful process and device optimization, 100X lower off-state leakage current with reasonable Ion was achieved comparing to previously reported values. Off-state leakage current presented in this work is suitable for 45nm LSTP application and beyond.

- Isolation & Well formation
- Gate Stack Formation (see Fig. 2)

		SiO_2	HfO_2	HfSiO
IL	[nm]	2.5	0.6~1.9	1.0
High-k	[nm]	x	3 ~ 5	3 ~ 4
Gate		TiN or TiSiN / poly-Si		
Etch & Cleaing		Wet or Dry		

- N & P LDD/halo I/I
- Nitride spacer (90nm)
- N & P SD I/I
- SD RTA ILD & Contact formation
- Metallization & Forming Gas Anneal (480ºC, 30min)

Fig. 1. Process Flow of CMOS fabrication.

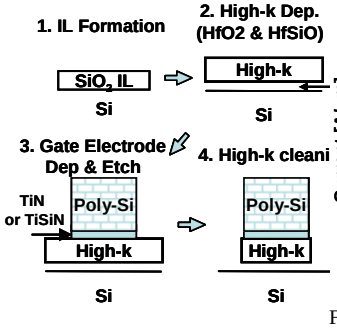


Fig. 2 Schematic diagrams of gate stack formation and split conditions

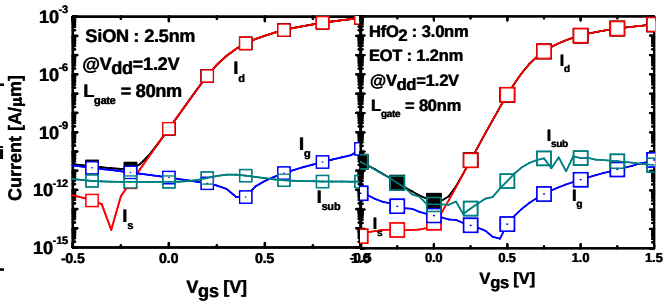
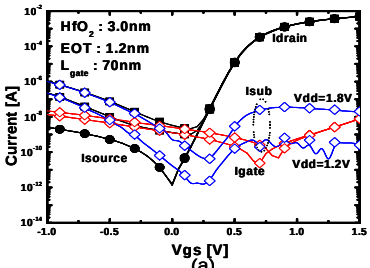
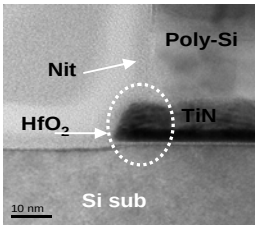
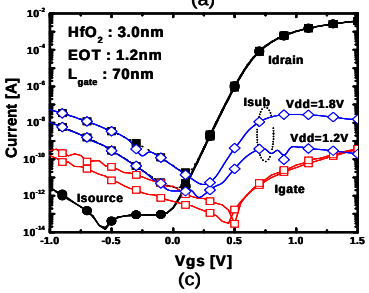


Fig 3. Typical GIDL characteristics for SiON vs. HfO_2. Due to the significant decrease of gate leakage current, transistor off current was also decreased for high-k device.







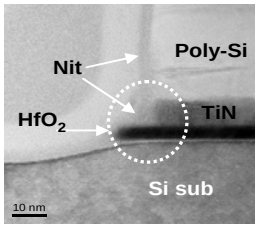


Fig. 4. GIDL characteristics with different gate edge profiles. (a) and (b) represent I-V characteristics and corresponding TEM image for just etched gate edge profile, respectively. (c) and (d) are I-V curve and TEM for the protruded high-k structure, respectively.

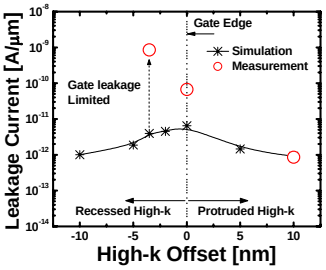


Fig. 5. Dielectric recess effects on leakage currents.

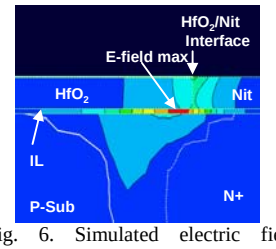


Fig. 6. Simulated electric field contour. E_{mmax} was located gate overlap region indicating that GIDL increases with the intermediately recessed high-k profile.

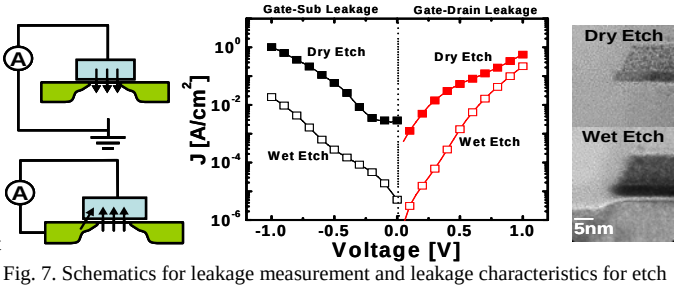


Fig. 7. Schematics for leakage measurement and leakage characteristics for etch process condition with corresponding TEM pictures.

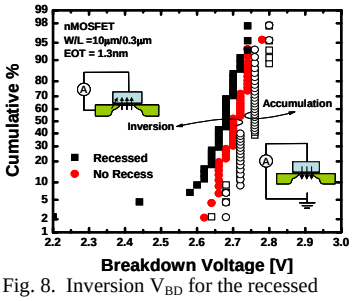


Fig. 8. Inversion V_{BD} for the recessed high-k structure was decreased.

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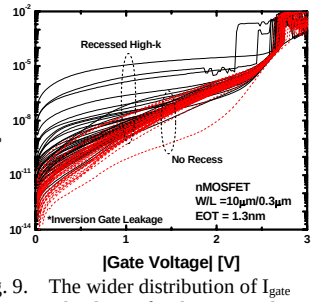


Fig. 9. The wider distribution of I_{gate} appears to be due to for the recessed structure.

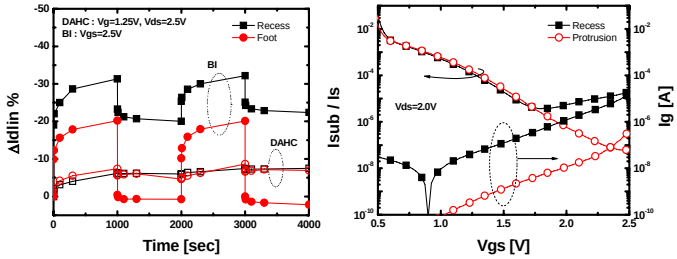
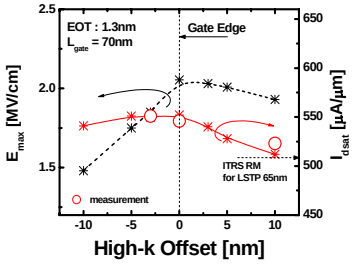
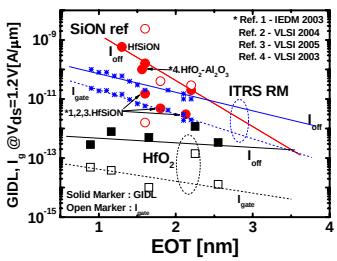


Fig. 10. I_{dlin} variation under DAHC and BI stress. For DAHC, the both devices degrade identically. Unlikely the recessed device, however, the degradation in the protruded device is fully recoverable under BI stress.





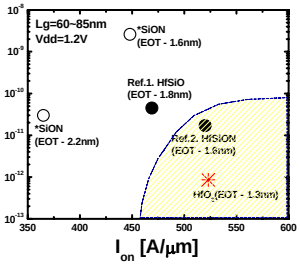


Fig. 11. For the protruded structures, Ion was decreased about 5% due to the reduced LDD doses.

Fig. 12. Leakage current and standby power comparison between this work and references.

REFERENCES

[1] T. Iwamoto et al, IEDM Tech. Digest, p.639, 2003.

[2] Y. Yasuda et al, VLSI Tech Symp., p40, 2004.

[3] M. Terai et al, VLSI Tech Symp., p.68, 2005.

[4] C. B. Oh et al, VLSI Tech Symp., p.71, 2003

[5] CHAN, T. Y. et al., , IEDM Tech Digest pp. 718-721,

[6] J. A. Mandelman, et al., IBM J. RES. & DEV. VOL. 46 NO. 2/3 MARCH/MAY 2002

[7] C. Y. Kang et al., Appl. Phys. Lett. 86, 123506 (2005)