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Compatibility of ALD Hafnium Silicate with Dual Metal Gate CMOS Integration

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Abstract

The compatibility of atomic layer deposited (ALD) hafnium silicate (HfSiON) with a deposition-etch-deposition based dual metal gate CMOS integration process has been systematically studied. Several *n*-MOS candidate metal gates were deposited by different deposition techniques such as physical vapor deposition (PVD), chemical vapor deposition (CVD) and ALD followed by selective wet etching process. Then, Al_2O_3 followed by CVD TiN was deposited to achieve a metal gate *p*-MOSFET. The fabricated device performance was compared with the same gate stack directly deposited without any wet etch. It was found that the device performance does not degrade as a result of the selective *n*-MOS metal gate wet etching process. This shows that ALD HfSiON is a compatible high-k dielectric film for dual metal gate CMOS integration. Dry etch for selective metal gate removal is also investigated, showing appropriate etch chemistry and bias condition allow negligible damage on the HfSiON.

Introduction

The introduction of high-k gate dielectrics has taken longer than originally envisioned. To date, ALD HfSiON has emerged as the most physically and electrically stable high-k material [1]. Several gate first dual metal gate integrations have been reported on HfO_2 [2, 3]. While HfSiON has been identified as a scalable and stable high-k material with respect to equivalent oxide thickness (EOT) and gate leakage [4], no detailed study has been reported to study its compatibility with dual metal gate fabrication processes, especially due to its vulnerability to HF based chemistries. Although, different techniques have been demonstrated to integrate dual metal gate CMOS, there is no agreement on the best scheme for HfSiON integration with metal gates. A deposition-etch-deposition scheme (Fig. 1) has shown the greatest flexibility of all the demonstrated techniques. However, since the scheme includes metal deposition and subsequent metal wet etch on high-k dielectric film, these processing steps may have an impact on the underlying high-k dielectric. In this letter, a focus experiment has been made to study the compatibility of ALD HfSiON with the critical multi-step integration processes.

Experimental

p-MOSFETs were fabricated using a deposition-etch-deposition based dual metal gate CMOS process flow (Fig. 2) with a thermal budget of 1070ºC conventional spike anneal after the source/drain implantation. A pre gate clean was performed using diluted HF before atomic layer deposition of 2 nm HfSiON, followed by a post-deposition anneal (PDA) at 700°C in NH_3 ambient. Afterwards, different potential metal electrodes for *n*-MOSFETs – tantalum silicon nitride (TaSiN), Titanium Nitride (TiN) and hafnium Silicide ($HfSi_x$) were deposited by PVD, ALD and CVD, respectively [5]. Then the deposited metals were selectively etched with standard cleaning agent SC1 (H_2O: H_2O_2: NH_4OH) and NH_4OH at an elevated temperature (~ 50 °C) to simulate a-Si hard mask etch. In another split, HfSiON films underwent simulated chemical wet etch, without actual metal gate or amorphous silicon (a-Si) hard mask deposition. For all the wafers, 1 nm of aluminum oxide (Al_2O_3) was deposited by ALD, followed by chemical vapor deposition (CVD) of 20 nm titanium silicon nitride (TiSiN) to form *p*-MOSFET. 100 nm of poly silicon was deposited and patterned with a plasma based dry etch to form the HfSiON/Al_2O_3/TiSiN gate stack. Performance characteristics of the as deposited *p*-MOSFETs without any wet chemical treatment was compared with MOSFETs fabricated after metal deposition and wet etch or simulation etch.

Results and Discussion

The electrical performance of the as deposited gate stack and the wet chemical treated stacks were compared in the context of effective oxide thickness (EOT), gate leakage (J_g), threshold voltage (V_t), short channel effects (SCE), transistor characteristics, hole mobility and interface state density (N_{it}). It was found that wet chemical etch itself did not reduce EOT in HfSiON films (Fig. 3). It was previously reported that in the case of HfO2 there is some EOT loss due to metal deposition and subsequent wet etch [6]. A small reduction in EOT for PVD TaSiN may be attributed to the PVD related bombardment and hence metal/high-k interface loss. Use of amorphous silicon hard mask gives the flexibility to use non-HF based chemistry, which is benign to relevant high-k dielectric films and metals. Typical oxide based hard mask would not be compatible as the hard mask removal process chemistry will etch the underlying high-k dielectrics also. Despite small EOT variation, J_g in all the wet etched devices were less than the control wafer (Fig. 4). This may be attributed to carbon removal by wet treatment from the high-k surface. Although, flat band voltage (V_{fb}-) was same for directly deposited and simulated wet etch sample – there was a minor difference whenever any metal is deposited and wet etched. This indicates that metal deposition has a small effect, causing a V_{fb} shift of 0.02V. Excellent within wafer distributions of linear V_t of 10x1 μm *p*-MOSFETs were obtained, indicating a uniform wet etch process (Fig 5). Moreover, long channel V_t for devices processed after metal deposition and etch or after a simulated wet etch were identical to the as-deposited control wafers. Fig. 6 shows the V_t roll-off characteristics of *p*-MOSFETs with CVD TiSiN metal gate electrodes that had various *n*-type metal gate electrodes ($HfSi_x$, TiN, TaSiN) and wet etched. As Fig. 6 shows, all the metals exhibits a normal V_t roll-off. The charge pumping results measured on 10x1 μm *p*-MOSFETs show that all the experimental *p*-MOSFETS had N_{it} comparable to the control wafer (Fig. 7). In contrast, the N_{it} values increased for PVD metal gates, due to the physical nature of the PVD process. The mobility values were somewhat degraded for all *p*-MOSFET devices, (Fig. 8). This is likely related to Al diffusing into the high-k/silicon substrate interface, which is known to degrade mobility (Fig. 9). However, the ALD metal deposition and etch sample showed similar mobility as that of the control as-deposited wafer which is consistent with its slightly higher EOT. It appears that the wet chemical simulated sample suffered a slightly degraded mobility may be because of NH_4OH induced silicate loss originated surface roughness of HfSiON (Fig. 10). AFM measurement shows that R_{rms} goes up from 0.13 nm to 0.17 nm. Due to the concern on the metal undercut in wet etch process, selective metal dry etch process also investigated stop on the high-k. Fig. 11 compares C-V curves of as deposited ALD TiN and re-deposited TiN after dry etch using HBr chemistry. Both just-etched (EPD+0%) and over etched samples (EPD+100% OE) show almost identical C-V curves to as-deposited device, indicating that the selective dry etch process also can be implemented without significant damage to the HfSiON.

Conclusion

A comprehensive, thorough study has been made to investigate the compatibility of HfSiON dielectric with the deposition-etch-deposition based dual metal gate CMOS integration process. It was found that in spite of first metal deposition and wet etch the performance does not degrade for ALD Al_2O_3/CVD TiSiN based metal gate *p*-MOSFETs on HfSiON dielectric in comparison to devices where the same metal has been directly deposited. Therefore, HfSiON is compatible with dual metal gate CMOS integration process. Dry etch for selective metal gate removal is also promising to prevent damage to the high-k as well as metal undercut if appropriate chemistry and bias conditions are selected.

Reference

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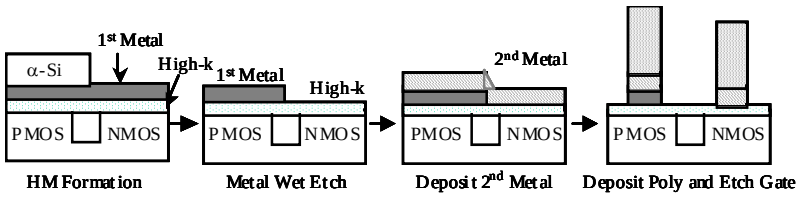

Fig. 1 Outline of the deposition-etch-deposition based dual metal gate CMOS flow utilizing a metal wet etch module. First metal and hard mask is deposited; patterned; metal wet etch of first metal from the open area; hard mask removal and 2nd metal deposition; poly deposition; gate pattern.

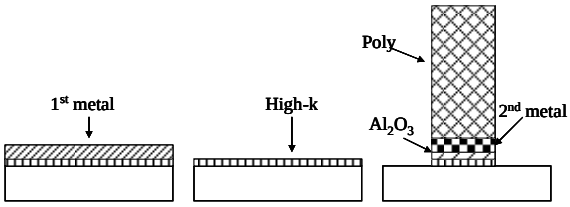

Fig 2. Experimental flow: deposition of HfSiON and PDA; first *n*-MOS metal deposition; metal wet etch; Al2O3 and CVD TiSiN deposition to achieve *p*-MOS metal electrode; poly-Si deposition; gate etch.

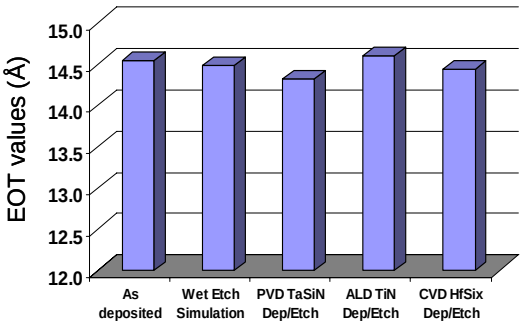

Fig. 3 EOT variation graph shows only the PVD metal deposition and etch lost EOT.

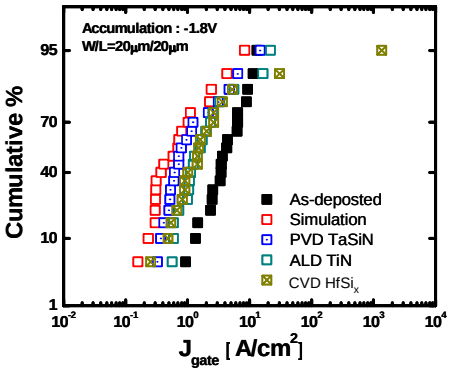

Fig. 4 Reduced Jg was observed for wet etched samples in accumulation.

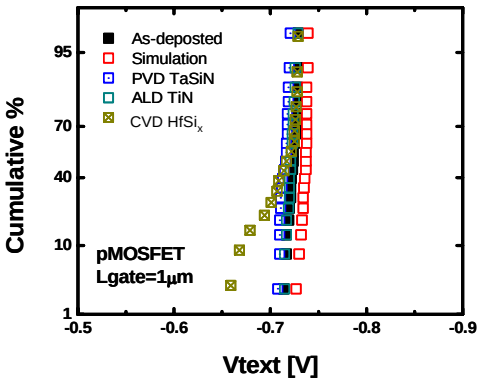

Fig.5 Excellent within wafer distributions of linear Vt of 10x1 mm *p*--MOSFETs indicates a uniform wet etch process

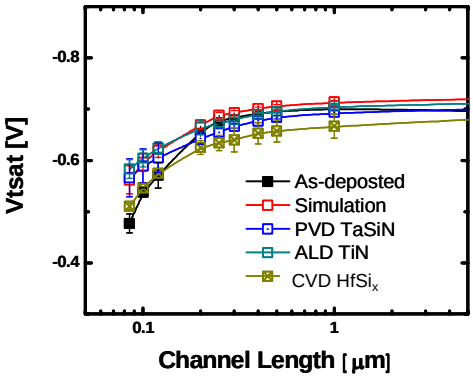

Fig. 6 Vt roll-off characteristics of experimental devices show similar roll-off.

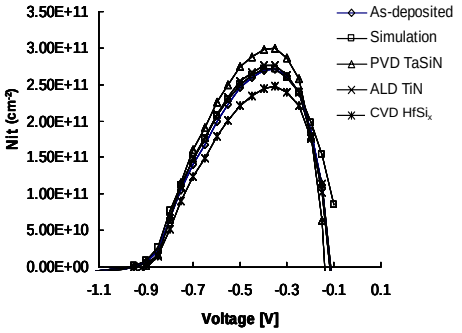

Fig. 7 The charge pumping results measured on 10x1 mm *p*--MOSFET show that all the experimental *p*-MOSFES had comparable Nit.

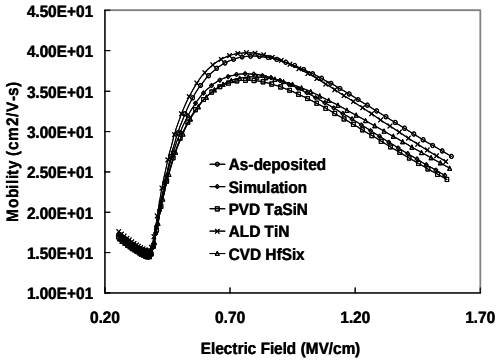

Fig. 8 Due to Al2O3 overall *p*-MOSFETs mobility is little degraded.

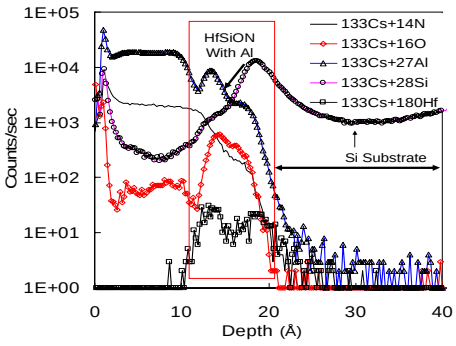

Fig. 9 Due to downward diffusion of Al into the HfSiON, hole mobility is degraded.

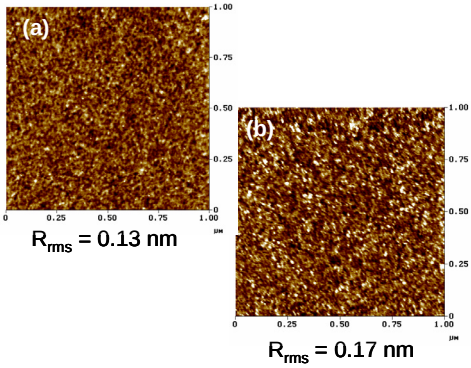

Fig 10 AFM shows (a) as-deposited HfSiON roughens a little (b) after wet etch

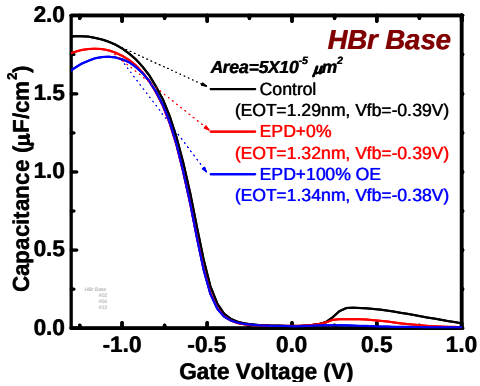

Fig 11 C-V curves of as deposited ALD TiN and re-deposited TiN after dry etch using HBr chemistry.