J-8-5
Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Yokohama, 2006, pp. 1116-1117

Full-Metal-Gate Integration of Dual-Metal-Gate HfSiON CMOS Transistors by Using Oxidation-Free Dummy-Mask Process

F. Ootsuka, Y. Tamura(*1) , Y. Akasaka(*2) , S. Inumiya, H. Nakata, M. Ohtsuka,
T. Watanabe, M kitajima, Y. Nara and K. Nakamura(*3)

Semiconductor Leading Edge Technologies, Inc. (Selete), 16-1 Onogawa, Tsukuba-shi, Ibaraki, Japan
TEL: +81-29-849-1260, FAX: +81-29-849-1186, E-mail: ohtsuka.fumio@selete.co.jp

Abstract

Full-metal-gate HfSiON CMOSFETs with W/TiN and W/TaSiN gate stacks have been successfully fabricated. We have developed a new dummy mask process that minimizes gate over-etch damage and suppresses any deterioration of n- and p-metal caused by oxidation. The electrical characteristics obtained for these dual-metal gate transistors are almost the same as those for single-metal gate transistors. The operation of the CMOS ring oscillator with full-dual-metal gate transistors is reported for the first time.

Introduction

Metal gate electrodes are beneficial in eliminating depletion layers in gate electrodes, resulting in a larger inversion capacitance. In addition, if combined with a high-k gate dielectric with a smaller equivalent oxide thickness (EOT), larger current drivability than is achieved with conventional poly-Si/SiON gate stacks can potentially be obtained. However, dual-metal gates with different work-functions are needed in order to reduce threshold voltage (V_{TH}) for both nFETs and pFETs if one considers their application to low operating power (LOP) and high performance (HP) devices.

Up to present, CMOSFETs with dual-metal gates consisting of poly-Si/metal have been reported [1,2]. Pure metal cladding layers are more desirable for scaled devices rather than poly-Si, if the aim is to reduce gate resistance. The occurrence of over-etch damage at the Si surface during gate etching is a great concern if gate stacks with different heights for nFETs and pFETs are employed as was reported in [1,2] and which are etched simultaneously. Another concern is excessive oxidation of the metals during mask layer deposition or the photo-resist ashing processes, since this deteriorates the metal properties that define their work-functions. We have developed a new dummy mask process that can avoid these problems, and the electrical characteristics of the CMOS transistors fabricated by this process are described in this paper.

Device Fabrication

Fig.1 shows the process flow of the new dual-metal gate process with the dummy mask layer. After isolation and ion implantations, HfSiO is deposited by MOCVD, followed by plasma nitridation and post-nitridation annealing [3]. A TiN p-metal layer and an initial SiN mask layer are deposited by CVD. The 1st SiN mask is then removed by dry etching in the p-well regions. After ashing the photo-resist, the exposed TiN is removed by an H_2O_2 wet treatment. A TaSiN n-metal layer is then deposited by a reactive sputtering, followed by deposition of the 2nd SiN mask layer. The 1st and 2nd masks are deposited by CVD using Si_2Cl_6 and NH_3 at 450^{o}C, which avoids excessive oxidation of the work-function metals. The 2nd SiN mask and the TaSiN are removed by dry etching in the n-well regions. The remaining SiN mask layers are etched off using dHF wet treatment. Neither TiN nor TaSiN is damaged because the SiN masks deposited at low temperature are very fragile against dHF and easily removed. We next sputtered 50nm-thick W layer to reduce the gate resistance and deposited a SiN hard mask. The etching of the gate electrodes for the nFETs and pFETs was performed simultaneously. By following this process flow, over-etch damage at the Si surface can be minimized. Fig.2 shows an SEM bird's-eye view after gate etching. Cross-sectional TEM images of the gate stacks are shown in Fig.3. The gate electrodes are surrounded by the SiN hard mask and sidewall spacers. The use of the resist in stead of the 2nd SiN in the TaSiN removal process is another choice. However, HfSiON is heavily oxidized in the ashing process, resulting in the increase of EOT (Fig.4). The use of SiN mask can avoid this excessive oxidation. After the S/D ion implantations, activation annealing was carried out at 1000^{o}C. NiSi was used for the salicidation process.

Comparison of Electrical Characteristics in CMOSFETs between Single- and Dual-Metal Gate Flow

One of the issues affecting this process is whether or not the HfSiON that is used for the nFETs is degraded by the TiN removal process. Fig.5 shows the gate leakage currents of FETs fabricated using the single- and dual-metal gate flows. Here, the single-metal gate flow means that W/TaSiN or W/TiN is deposited after HfSiON formation without TiN removal. The nFETs in the dual-metal flow exhibit larger gate leakage current than those of single-metal. In the case of pFETs, W/TiN is deposited immediately after HfSiON formation, and hence, HfSiON is not processed through TiN removal sequence. Furthermore, a larger gate capacitance is observed for nFETs using the dual-metal flow than is observed for the single-metal flow (Fig.6). These results imply that the surface of the HfSiON is etched slightly during the TiN deposition and the removal sequence. The decrease in EOT caused by TiN removal is about 0.1nm (Fig.7). In spite of the decrease in EOT, Jg is smaller than that for SiO_2 by four orders of magnitude, and is on the trend line of the Jg-EOT of nFETs even at sub-1nm EOT. The dependence of carrier mobility on the effective electric field in the inversion layer is shown in Fig.8. Compared with FETs in the single-metal flow, no mobility degradation is observed for either nFETs or pFETs in the dual-gate flow. Furthermore, we evaluated the device reliability of full-dual-metal gate nFETs under positive bias temperature stressing (Fig. 9). There was no obvious difference between the single- and the dual-metal flows.

Device Performance of CMOSFETs with Dual-Metal

We have obtained excellent electrical characteristics for the HfSiON CMOS transistors with 0.84nm EOT which are fabricated by using the dummy mask process. Fig.10 shows the V_{TH} roll-off characteristics for nFETs and pFETs. The FETs are operational at the gate length of 65nm, and almost symmetrical V_{TH} values are obtained for nFETs and pFETs without counter-channel implantation. Fig.11 shows the Ion-Ioff characteristics at 1.1V supply voltage. Ion is 710μA/μm for nFETs and 340μA/μm for pFETs at 100nA/μm Ioff. A CMOS ring oscillator constructed with full-dual-metal gate transistors is operational (Fig.12) and 26psec inverter-delay has been obtained at the gate length of 65nm (Fig.13).

Conclusion

We demonstrated the characteristics of HfSiON CMOS transistors with full-dual-metal gates consisting of W/TaSiN and W/TiN stacks. Transistors are fabricated by a dummy mask process, which minimizes a gate over-etch damage and suppresses deterioration of the n- and p-metals. The electrical characteristics obtained for the dual-metal gate transistors are almost the same as those for single-metal-gate transistors. The operation of the CMOS ring oscillator with full-dual-metal gate transistors is reported for the first time.

References

[1] S. B. Samavedam, et al., IEDM Tech. Dig. 2002, p.433
[2] Z. B. Zhang, et al., 2005 Symp. VLSI Tech. Dig., p.50
[3] S. Inumiya, et al., IEDM Tech. Dig. 2005, p.27

Present affiliation: (*1)Fujitsu Labs. Ltd., (*2)Tokyo Electron Ltd., (*3)NEC Electronics Corp.

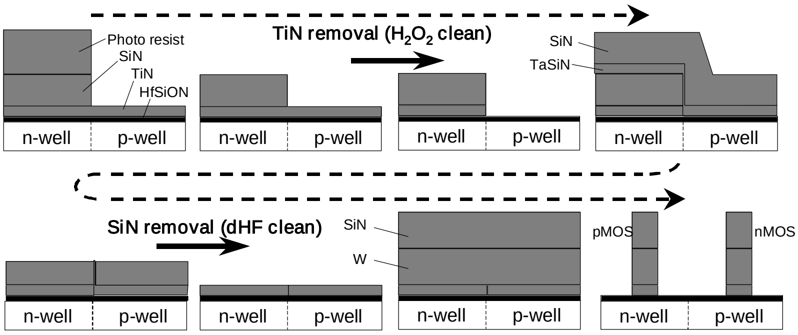

Fig.1 Schematic cross-section of dual-metal gate process flow.

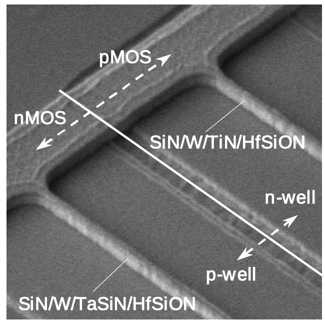

Fig.2 SEM bird's-eye view of W/TiN/HfSiON and W/TaSiN/HfSiON gate stacks after gate etching process.

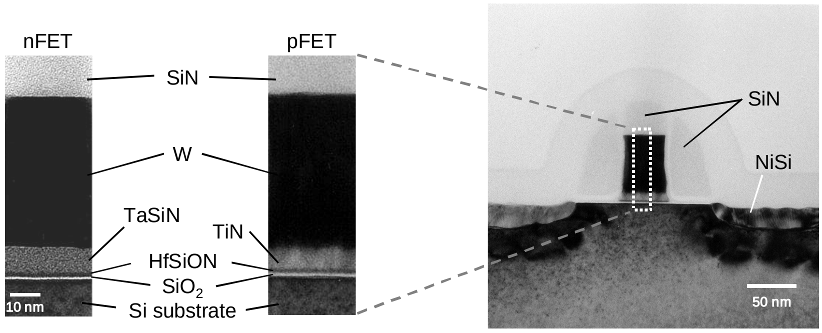

Fig.3 Cross-sectional TEM images of gate stacks of nFET and pFET.

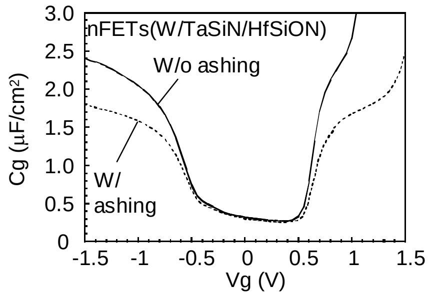

Fig.4 Change in Cg-Vg due to ashing process after SiN wet-removal.

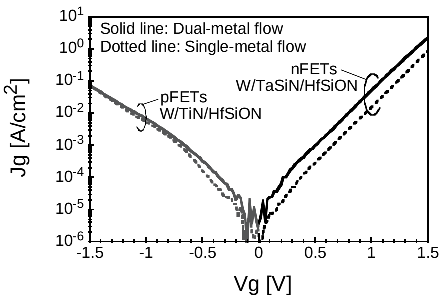

Fig.5 Jg-Vg characteristics of nFETs and pFETs fabricated by single- and dual-metal gate process flow.

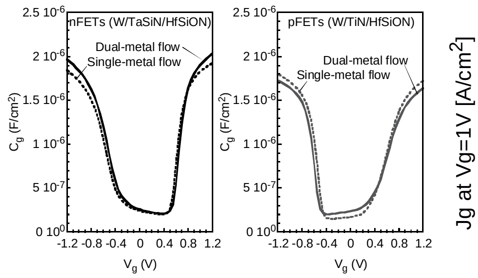

Fig. 6 Cg-Vg characteristics of nFETs and pFETs fabricated by single- and dual-metal gate process flows.

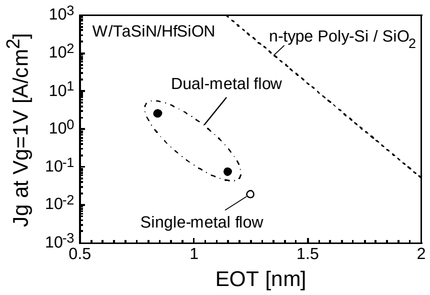

Fig.7 Gate leakage current as a function of EOT for nFETs fabricated by single- and dual-metal gate flow.

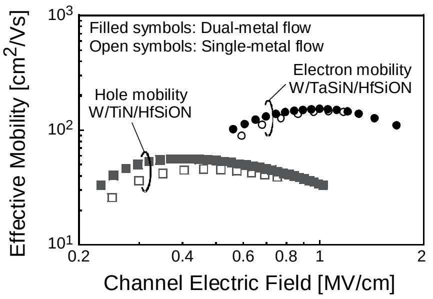

Fig.8 Electron and hole mobility for nFET and pFET, respectively.

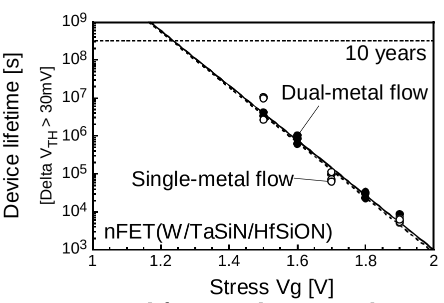

Fig. 9 Device lifetime under positive bias temperature stressing for nFETs fabricated by single- and dual-metal gate flow.

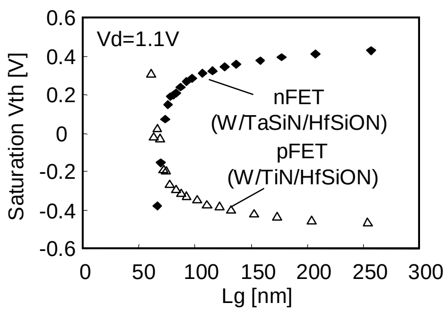

Fig.10 Vth roll-off of dual-metal-gate CMOS.

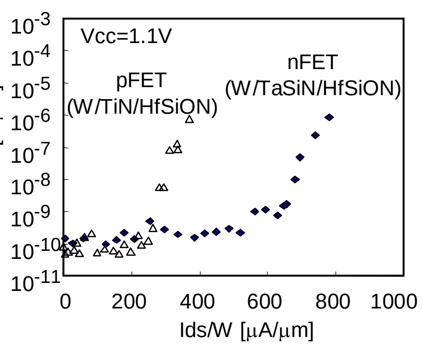

Fig.11 Ion-Ioff of dual-metal-gate CMOS.

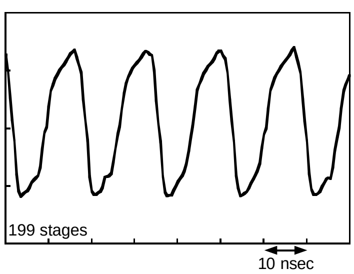

Fig.12 Ring oscillation characteristics of full dual-metal gate CMOS transistors.

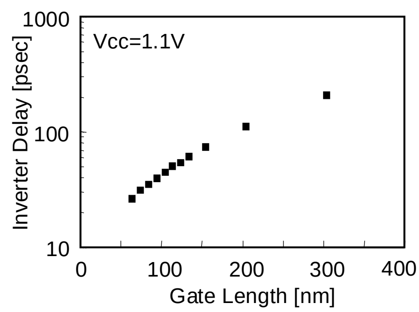

Fig.13 Inverter delay as a function of gate length for full dual-metal CMOS transistors.