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Degradation and Breakdown of Sub-1nm EOT HfO_2/Metal Gate Stacks

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1. Introduction

Due to the exponential increase in leakage current when scaling down the gate oxide thickness of MOSFETs, there is an urgent need to replace SiO_2-based dielectrics by high-k dielectrics. One of the candidates that allow sub-1nm EOT is HfO_2. Not only gate leakage current decrease, but also performance parameters (drive current, mobility) need optimization. Moreover, it is very important to guarantee sufficient reliability for these new types of gate stack.

In this paper, we review our present understanding of the degradation and breakdown (BD) of technologically relevant sub-1 nm HfO_2 under electrical stress. We used nMOSFETs with W/L = 0.25 or 10 μm/0.5 or 10 μm. The 0.9 nm EOT ALD-HfO_2/TaN gate stack shows state-of the-art electric performance [1]

2. Trap generation and degradation model

HfO_2 layers suffer from a defect band close to the conduction band, especially when poly-Si gates are used [2]. These defects give rise to V_t-instability and C-V hysteresis. Using metal gates and scaling down the high-k physical thickness reduces the V_t-instability to acceptable levels.

Besides these initial defects, additional HfO_2 bulk traps are created during positive Constant Voltage Stress (CVS), leading to BD when a critical trap density is reached (as in SiO_2) [3]. In sub-1nm EOT high k layers, the generation of bulk HfO_2 traps can be observed in several ways:

1) First, the generated traps give rise to SILC (Fig. 1) that shows a power law increase with time with exponent ~0.7 (298 K) or ~0.8 (398 K). At 398K, the SILC voltage acceleration at a sense voltage of 1 V (Fig. 2) can be fitted well with the recently published [4] power law voltage acceleration law ($t=t_0.V_G^n$) with n=-24 (or n=-28 at 298 K).

2) On very small samples ($1.25\text{-}5x10^{-9}$ cm^2) we can actually observe the creation of an individual leakage path corresponding to the creation of an individual trap [5]. If we 'count' the number of generated traps as a function of stress time a power law is found with exponent ~0.35 (Fig. 3), half of the value of the SILC power law exponent, while the voltage acceleration exponent n=-24 is within error bar identical to the SILC voltage acceleration exponent (Fig. 4).

3) The bulk HfO_2 trap generation can also be measured by variable frequency Charge Pumping [3]. Again a power law increase of the trap density vs. time is seen (Fig. 5) with exponent ~0.4. The V_G-acceleration has n=–31 (Fig. 6).

Linking the results of the three characterization methods discussed above, a consistent picture emerges of the degradation of HfO_2. Indeed, from the similarity in both time and voltage dependence of the trap generation (fig. 5-6) and the generation of leakage paths (Fig. 3-4), it can be concluded that the creation of each single HfO_2 bulk trap is causing a trap-assisted leakage path in the dielectric, which gives rise to the small single trap current increases (1-100pA). After more time, more conducting (~10nA-1mA) two trap percolating clusters form, causing the SILC in Figs 1-2. This is confirmed by the fact that SILC has the same voltage acceleration as the trap generation (Fig. 2 and 6), but twice the time power law exponent (0.7 for SILC vs. 0.35 for trap generation).

3. Time-Dependent Dielectric Breakdown (TDDB)

In very small devices the creation of a two-trap percolation cluster is interpreted as a soft BD (SBD). This means that the SILC in Fig. 1 can also be interpreted as being caused by *multiple* SBDs. Consistent with theory [6], the SBD Weibull distribution (Fig. 7) has a slope of ~0.7, identical to the SILC power law exponent.

In stacks with *metal* gates the SBD develops after some wear out time into an abrupt hard BD (HBD) [7]. This is different to the case of *poly-Si* gates where a slow wear out ends with a gradual current run away [8]. The different evolution of the BD path conductivity in metal and poly-Si gated devices is probably due to the difference in the ballasting resistance that limits the positive feed-back mechanism that controls the SBD to HBD transition.

We found that the time *between* SBD and HBD can also be described by a Weibull distribution and consequently the HBD distribution is a *convolution* of two Weibull distributions (in case no multiple BD's occur) [9]. If the SBD is overlooked or ignored and the HBD distribution is approximated by a Weibull distribution, its slope will be voltage and area dependent (Fig. 8), leading to confusion and errors when predicting the stack reliability.

Correct low voltage extrapolations of t_{HBD} are done in 2 steps. 1) Determine t_{SBD} vs. V_G and use the conventional area and percentile scaling laws. 2) Add the leakage path wear out time $t_{wearout}$. The area scaling on t_{SBD} is, however, irrelevant at low V_G because $t_{wearout} >> t_{SBD}$, and the reliability can be determined directly by extrapolating t_{HBD} to low voltage without any area scaling! Because of the slow wear out phase, t_{HBD} for HfO_2 is sufficiently high at low voltage (fig. 9). The main reliability problem of these sub-1nm EOT high k/metal gate stacks is therefore the strong gate leakage current increase due to multiple SBDs.

4. Conclusions

We demonstrated that a 0.9 nm EOT ALD HfO_2/TaN gate stack can be intrinsically reliable for TDDB under CVS. During degradation, single traps and two-trap clusters are formed in the HfO_2, the latter giving rise to a considerable SILC. The two-trap clusters wear out with time leading to HBD, but at operating conditions this takes longer than the required lifetime. The main reliability issue for thin HfO_2 stacks is therefore the SILC, which has to be taken into account by circuit designers.

Acknowledgements

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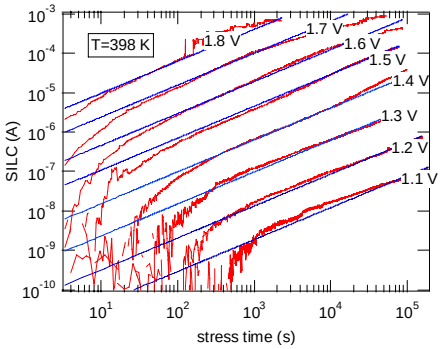

Fig. 1: SILC vs. time after eliminating the charge trapping effect (only shown at 398 K). After the transient part, a power law can fit the curves with a constant exponent of 0.7 (298 K) or 0.8 (398 K).

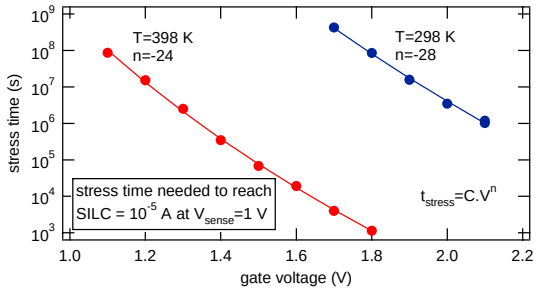

Fig. 2: The SILC voltage acceleration can be fitted well with a power law. Especially at 398 K, the data are in a sufficiently wide V_G range to allow a clear discrimination between a linear (log(t) vs. VG) and power law.

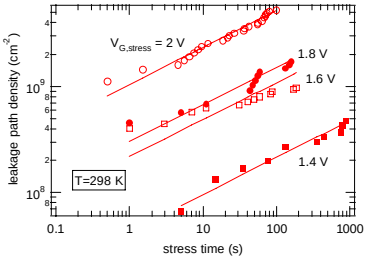

Fig. 3: The generation of leakage paths vs. stress time can be fitted with a power law with exponent 0.35.

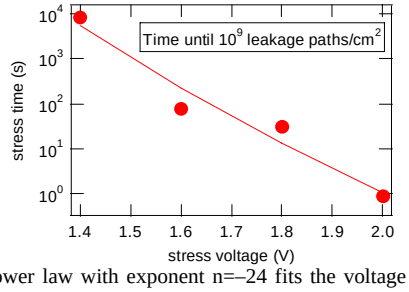

Fig. 4: A power law with exponent n=–24 fits the voltage acceleration of the generation of leakage paths.

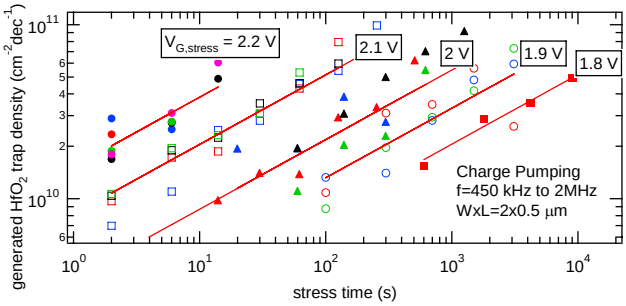

Fig. 5: The increase of the HfO_2 bulk trap density extracted from variable frequency charge pumping measurements. A power law with an exponent of approximately 0.4 fits the data satisfactorily.

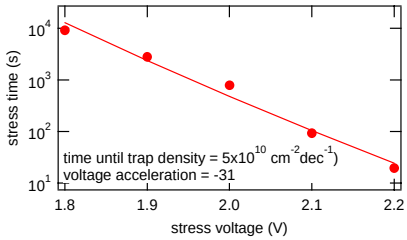

Fig. 6: The voltage acceleration of the trap generation process measured by charge pumping. A power law fit results in exponent n =-31.

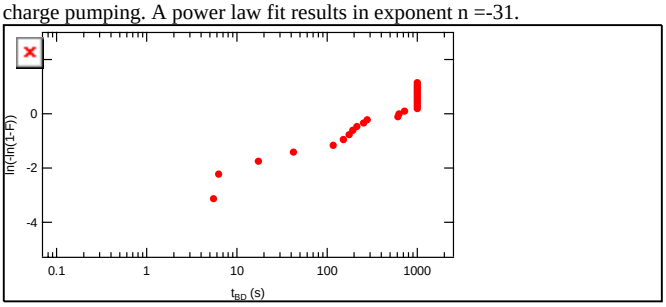

Fig. 7: The distribution of the first created conduction path with current >5x10^{-8}A at stress condition (i.e. soft BD). These distributions have a slope of 0.7-0.8, indicating the formation of two-trap clusters. Vertical columns of data are time-outs (and not BDs), which are consistently included in the Weibull fitting algorithm.

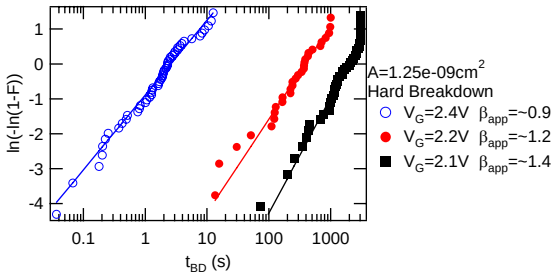

Fig. 8: The change of the shape of the apparent Weibull distribution for HBD. As the V_G decreases, distribution appears steeper. Vertical columns of data are time-outs.

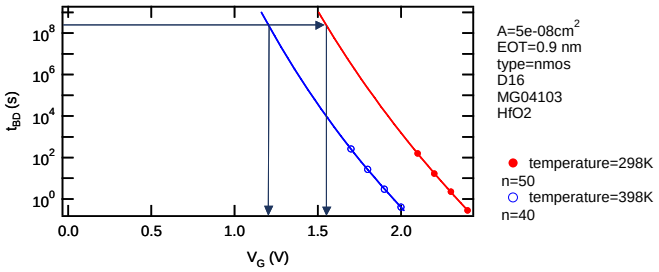

Fig. 9: Low voltage extrapolation of t_{HBD} results in sufficient lifetime for 0.9 nm HfO_2 both for 298 K and 398 K. A power law extrapolation was used with exponent ~50 at 298 K and ~40 at 398 K. Maximum operating voltage at 10 years is ~1.6 and ~1.2 V respectively.

References:

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