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Impact of Captured-Carrier Distribution on Recovery Characteristics of Positive- and Negative- Bias Temperature Instability in HfSiON/SiO_2 Gate Stack

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Introduction

Bias temperature instability (BTI) lifetime under the AC stress contains the process of not only degradation but also the recovery[1-3]. Therefore, the recovery ratio is key concern in the lifetime under the real operation condition. In this study, the recovery processes of positive- and negative- bias temperature instability (PBTI, NBTI) in HfSiON were examined in detail. As a result, it was found that the recovery process of BTI degradation depends on interfacial layer thickness and electric field across HfSiON/SiO_2 stack. It is concluded that the recovery process strongly relates to the balance of captured electrons and holes in the gate insulator.

Experimental

The devices used in this study were n+poly/n-MISFET and p+poly/p-MISFET with HfSiON (Hf/(Hf+Si)=50%, [N]=20%) dielectrics fabricated by MOCVD method. The dimension of MISFET is 10μm gate width and 1μm gate length. The physical thickness of gate HfSiON film and SiO_2 interfacial layer (IL) were shown in Table 1. Fig.1 shows the schematic diagram of stress sequences. Unipolar stresses were applied. Threshold voltage (Vth) and generated interface-states (Dit) are estimated by Id-Vg measurement and charge-pumping measurement during respective stress.

Results and Discussion

Fig.2 shows the time dependence of total threshold voltage shift (ΔVth) and threshold voltage shift originated in Dit ($\Delta Vth_{interface}$)[4] under unipolar PBT stress in n-MISFET of the sample with 1nm IL and that with 2nm IL. Note that ΔVth after PBT stress recovered by removing the stress. This degradation and recovery of ΔVth is repeated during unipolar stress. This result suggests that ΔVth under PBT stress contain the reversible process. The degradation and recovery of ΔVth are caused by the capture and the discharge of charges in bulk because $\Delta Vth_{interface}$ remain unchanged during unipolar PBT-stress. The recovery of ΔVth after PBT stress is clearly observed irrespective of applied PBT stress biases. Furthermore, the recovery of ΔVth for the sample with 2nm IL is smaller than that with 1nm IL (Fig.3). Fig.4 shows -ΔVth and $-\Delta Vth_{interface}$ under unipolar NBT stress in p-MISFET with 1nm IL and that with 2nm IL. The degradation and recovery characteristics of -ΔVth strongly depend on IL thickness. In the sample with 2nm, -ΔVth increases monotonically during 1^{st} NBT stress and 1^{st} removing stress. Furthermore, the degradation and the recovery of -ΔVth are repeated after 1^{st} removing stress. These behaviors of -ΔVth under unipolar NBT stress are quite different from those under unipolar PBT stress as shown in Fig.2 and 4. Fig.5 shows the characteristics of the degradation and the recovery under alternate different NBT-stress and removing the stresses. The recovery behavior of -ΔVth after NBT stress strongly depends on the stress biases and IL thickness. Furthermore, the monotonically increasing of -ΔVth after removing the stress was observed in both samples.

Fig.6 shows the stress field (Eox_stress) dependences of the recovery ratio extract from the data of Fig.3 and 5. The recovery ratio is defined as (ΔVth_recovery/ΔVth_stress) shown in Fig.6 (c). In n-MISFET, the recovery ratio of the sample with 1nm IL is higher than that with 2nm IL. These results indicate that the thick IL suppresses the discharge of electrons. It is thought that the degradation and recovery of ΔVth during unipolar PBT stress is caused by the capture and the discharge of electrons because electron current is dominant carrier and hole current hardly flows in n-MISFET (Fig.7 (a)). The recovery ratio of PBTI becomes larger with decrease of Eox_stress as shown in Fig.6 (a). This result indicates that the discharge of electron depends on Eox_stress. In NBTI, it was found that the recovery ratio becomes larger with increasing |Eox_stress| as shown in Fig.6 (b). Furthermore, the negative recovery ratio was observed at low stress bias in the sample with 2nm IL. It is thought that both electrons and holes contribute this complex recovery behavior of ΔVth after NBT stress because both electrons and holes injected under negative biases (|Eox|>5MV/cm) in p-MISFET (Fig.7 (b)).

On the basis of experimental results, the recovery processes of PBTI and NBTI are discussed. Table 2 shows the contribution of the capture and the discharge of electrons and holes to ΔVth. The recovery ratio of PBTI and NBTI are described by Eqs.(1),(2) in Table 2. In PBTI, it is thought that the recovery ratio depends on the capture and the discharge of electron shown in Eq.(1). On the other hands, the recovery ratio in NBTI depends on the capture and the discharge of both electrons and holes shown in Eq.(2). Note that the contribution of electrons and holes to ΔVth are reverse polarity. Therefore, the recovery ratio shows very small or negative in NBTI. From the results of Eox_stress dependence of the recovery ratio in PBTI, we expect the location of captured electrons contribute the process of electron discharge as schematically shown in Fig.8 (a). The captured electron near electrode under low stress field is thought to easily discharge by removing the stress. In NBTI, it is thought that the recovery ratio depends on the balance of discharge of electrons and holes. Especially, the large contribution of electron discharge is though to be the cause of small or negative recovery ratio. Note that the ratio of electron injection and hole injection is almost same in range of Eox_stress(Fig.7(b)). Therefore, the positive recovery ratio in Eox_stress= - 9MV/cm and the negative recovery ratio in Eox_stress= - 8MV/cm cannot be explained by the difference of the amount of injection of carriers. We expect the location of captured electrons and hole and the easiness of the discharge of electron contributes to the recovery ratio. The contribution of electron for ΔVth is large under low stress fields because the electrons capture near the substrate as schematically shown in Fig.8 (b) and electron is easy to be discharged rather than hole, resulting in Eox_stress dependence of recovery ratio in NBTI.

Conclusions

The recovery process of PBTI and NBTI in HfSiON was investigated in detail. As a result, it was found that the thick IL suppresses the recovery of BTI. Furthermore, it was found that the recovery characteristics are quite different between PBTI and NBTI because of the different contribution of charges. Especially, we need to treat carefully for field acceleration of lifetime projection under AC stress because the balance of the contribution of the electron and the hole changes greatly by the electric fields.

References

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Table.1 Physical thickness of interfacial SiO_2 layer fabricated by ISSG and HfSiON film used in this study.

	IL(SiO_2)	HfSiON
(a)	1 nm	4 nm
(b)	2 nm	4 nm

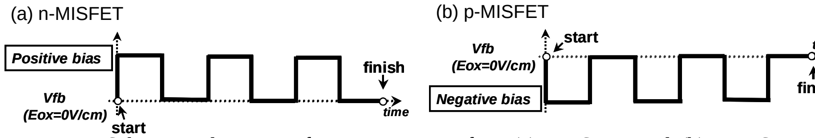

Fig.1 Schematic diagrams of stress sequence for (a)n-MISFET and (b) p-MISFET. Unipolar stresses were applied.

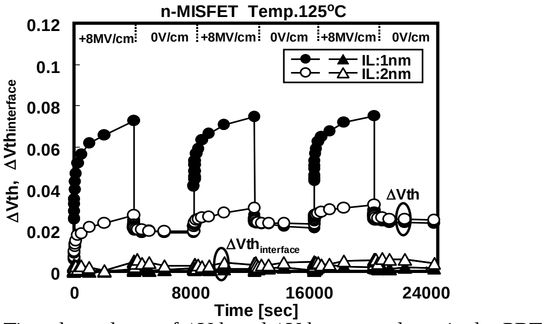

Fig.2 Time dependence of ΔVth and $\Delta Vth_{interface}$ under unipolar PBT stress in the sample with 1nm IL and that with 2nm IL. The degradation and the recovery of ΔVth are repeated during unipolar stress.

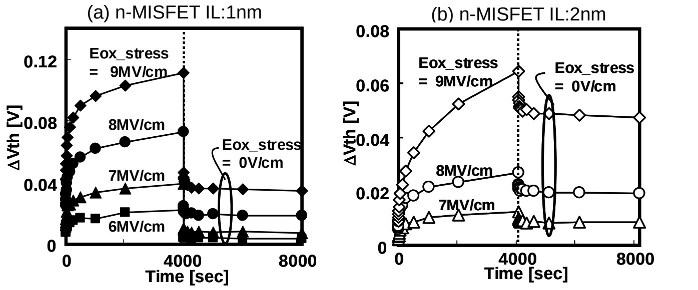

Fig.3 Time dependence of ΔVth in (a) the sample with 1nm IL and (b) the sample with 2nm IL of n-MISFET under alternate different PBT stress and Eox=0V/cm. The recovery behavior of ΔVth is clearly observed irrespective of stress field. Furthermore the recovery in the sample with 2nm IL is smaller than that with 1nm IL.

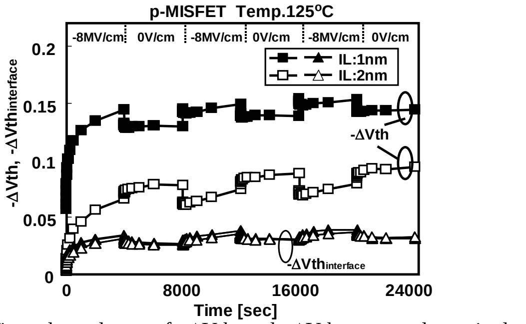

Fig.4 Time dependence of -ΔVth and $-\Delta Vth_{interface}$ under unipolar NBT stress in the sample with 1nm IL and that with 2nm IL. In the sample with 2nm, -ΔVth increases monotonically during 1st NBT stress and 1st removing stress. Furthermore the degradation and recovery of -ΔVth are repeated after 1st removing stress.

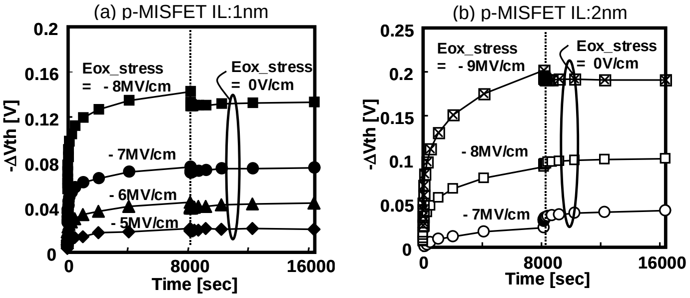

Fig.5 Time dependence of ΔVth in (a) the sample with 1nm IL and (b) the sample with 2nm IL of n-MISFET under alternate different NBT stress and Eox=0V/cm. The recovery behavior of ΔVth is strongly depends on stress fields and IL thickness. The recovery after NBT stress in p-MISFET is smaller than that after PBT stress in n-MISFET(Fig.3).

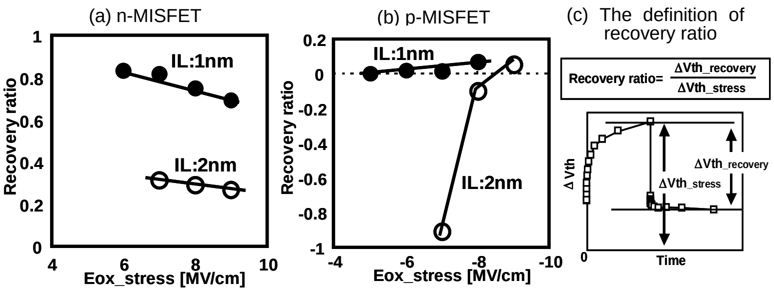

Fig.6 Stress fields (Eox_stress) dependence of the recovery ratio in (a) n-MISFET and (b) p-MISFET. The definition of recovery ratio is shown in Fig.(c). (a) In n-MISFET, greater recovery of ΔVth is possible for the sample with 1nm IL than that with 2nm IL. In addition it is found that the recovery progresses with decreasing Eox_stress.(b) In p-MISFET, the recovery ratio is becomes larger with increase |Eox_stress|. Furthermore, the negative recovery ratio is observed at low |Eox_stress| in the sample of 2nm IL.

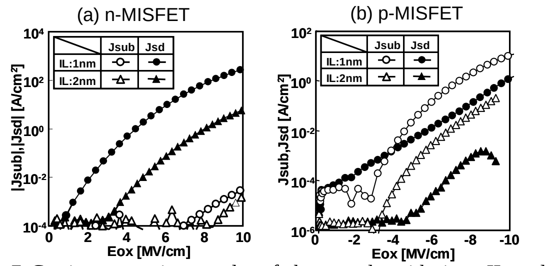

Fig.7 Carrier separation results of the sample with 1nm IL and those with 2nm IL in(a) n-MISFET and (b) p-MISFET. (a) In n-MISFET, the electron current (Jsd) is dominant carrier. The hole current (Jsub) caused by impact ionization is hardly observed. (b)In p-MISFET, both electrons current (Jsub) and holes current (Jsd) are observed. The amount of electron current is larger than that of hole current in both sample at |Eox|> 5MV/cm.

Table.2 The contributions of the capture and the discharge of electrons and holes to ΔVth. The recovery ratio in PBTI and NBTI can described by Eqs.(1) and (2). In Eq.(2), the contribution of Dit is small and negligible.

	electron	hole
capture	ΔVth (positive)	ΔVth (negative)
discharge	ΔVth (negative)	ΔVth (positive)

$$\text{Recovery ratio (PBTI)} = \frac{|\text{discharge of electron } (\Delta Vth(-))|}{|\text{capture of electron } (\Delta Vth(+))|} \quad \cdots (1)$$

$$\text{Recovery ratio (NBTI)} = \frac{|\text{discharge of hole}(\Delta Vth(+)) + \text{discharge of electron } (\Delta Vth(-)) + \text{decrease of Dit } (\Delta Vth(+))|}{|\text{capture of hole}(\Delta Vth(-)) + \text{capture of electron } (\Delta Vth(+)) + \text{increase of Dit } (\Delta Vth(-))|} \quad \cdots (2)$$

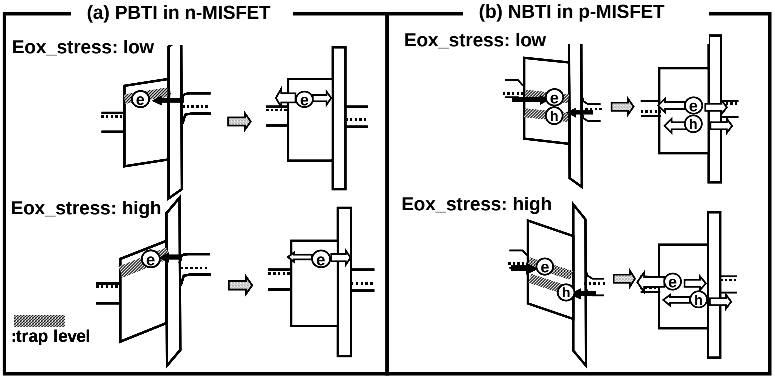

Fig.8 Schematic diagrams of (a)PBT and (b)NBT degradation and recovery for low stress bias and high stress bias. (a) In PBTI, we expect the location of captured electrons contributes to the discharge of electron, resulting in Eox_stress dependence of recovery ratio. (b) In NBTI, the location of both captured electrons and holes depend on Eox_stress. The contribution of electron for ΔVth is large when electrons capture near the substrate. Furthermore, it is thought that electrons are easy to be discharged rather than holes. These are the causes of small or negative recovery ratio in low stress bias.