Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Yokohama, 2006, pp. 1122-1123

J-9-3

Reliability of thick oxides integrated with $HfSiO_x$ gate dielectric

B. H. Lee[1,2], C.Y. Kang[1], T.H. Lee[3], J. Barnett[1], R. Choi[1], S.C. Song[1] and R.Jammy[2]

[1]SEMATECH, 2706 Montopolis Drive, Austin, TX, USA 78741, [2]IBM assignee
[3]University of Texas at Austin, USA
Phone: +1-512-356-3115, Fax: +1-512-356-3470, E-mail: byoung.hun.lee@sematech.org

1. Introduction

The research to implement the high-k dielectric is being accelerated. High-k gate dielectric with good mobility and EOT of 1nm has been demonstrated [1] and significant progresses are made in metal electrode implementation for dual workfunction CMOS application, including various integration schemes [2-5]. However, how these technologies can mix and match with existing CMO technologies has not been investigated systematically. For example, the multiple oxide scheme used to generate different threshold voltages for various devices is not easy to implement with high-k dielectric alone due to the difficulties in etch back of high-k dielectrics. Alternative is to combine thin high-k dielectric with multiple oxide structures, but unfortunately, high-k deposition is reported to affect the quality of interfacial oxide significantly by absorbing oxygen and forming sub-stoichiometric oxide [6]. If metal electrode/high-k dielectric gate stack would affect the quality of thick oxide, the reliability of I/O devices that use thick oxide could be degraded seriously.

To assess this problem, the reliability of gate dielectric system which has a high-k gate dielectric layer (~3nm) deposited on thick oxide in the range of 2nm-4nm is examined. Based on this result, favorable integration schemes combining thick SiO_2 and thin HfO_2 are suggested.

2. Sample fabrication

To simulate the multiple oxide structures with high-k dielectric, thin HfO_2 layer is deposited on thick SiO_2 layer. 2nm and 4nm of SiO_2 was grown using in-situ steam growth process and $HfSiO_x$ was deposited using ALD process. Thin thermal ALD TiN and MOCVD HfSix electrode (~10nm) capped with 100nm polysilicon layer are used as electrode. Fig.1 summarized the samples used in this work. After the gate stack formation, conventional CMOS flow with a 1075°C spike anneal is used to fabricate transistors.

3. Results and discussion

Mobility curves of various devices used in this work are shown in Fig.1. As the thickness of underlying oxide is increased, the impact of 3nm HfSiOx layer on mobility becomes negligible. 2nm SiO_2 layer appears to be enough to recover the high field mobility to the universal mobility curve. Interface state (Nit) measured at 100KHz to probe the Si-SiO_2 interface and its proximity region indicates that the influence of 3nm $HfSiO_x$ layer is similar for all samples, and N_{it} values are low enough to ignore. Thus, it can be concluded that thin $HfSiO_x$ deposited on multiple oxide region does not affect the quality of thick oxide in terms of interface states and mobility.

However, the threshold voltages of thick oxide device did seem to be affected by the presence of $HfSiO_x$ layer. Control TiN/SiO_2 and HfSi/$HfSiO_x$ devices showed tighter distribution than $HfSiO_x$/SiO_2 stack devices, indicating potential interactions between the HfSiOx and SiO_2 layer (Fig.3). This problem is more pronounced at PMOS side where the charges injected from gate electrode can be accumulated at the top interface between HfO_2 and SiO_2 and influence the V_{th}. On the other hand, NMOS side is relatively stable because the thick oxide layer suppresses the tunneling from the substrate. V_{th} distribution raises the concern about the reliability of total stack because typical reaction between high-k layer and SiO_2 is a reduction in SiO_2 layer and the reliability of oxygen deficient SiO_2 can be easily degraded.

Fig.4 show the time zero dielectric breakdown (TZDB) characteristics. The tight distribution of breakdown characteristics and negligible area dependence indicate that the TZDB process is an intrinsic characteristic of total gate stack (Fig.5, Fig.6). However, the breakdown field calculated from breakdown voltage divided by equivalent oxide thickness (EOT) of the gate stack showed more than 15MV/cm for SiO_2 portion in all samples. This is an abnormally high value for SiO_2. There are several ways to understand this result, but one straight forward way is to redistribute the bias by adjusting the dielectric constant of SiO_2 layer, assuming the dielectric constant of SiO_2 layer is increased by oxygen deficiency. Then, effective field in SiO_2 layer can be reduced to a reasonable level. Interestingly, 2nm SiO_2 sample showed the highest breakdown field, indicating the most reaction with HfSiOx layer.

Stress induced leakage current (SILC) and negative bias temperature instability (NBTI) are investigated because these tests are more sensitive to broken bonds in oxygen deficient SiO_2 gate dielectrics, which might mediate the leakage current or the hydrogen diffusion. It is not clear yet whether the constant field stress at 12MV/cm can be used to compare both single layer device and stack device, but qualitatively, the SILC characteristics of HfSiOx/SiO_2 stack are not degraded in comparison with TiN/SiO_2 sample. However, stacking of HfSiOx/SiO_2 seems to affect the NBTI characteristics significantly. While overall V_{th} shift is low, exponent values are deviated from typical SiO_2 value (n=0.16). Low exponent of sample A is due to the tunneling component in addition to hydrogen reaction and diffusion component.

Overall, the stacking of thin $HfSiO_x$ layer on multiple oxides region does not degrade the device performance such as mobility and Nit. However, the reliability is affected by the reaction between HfSiOx layer and SiO_2 layer. In this work, the effects of nitridation on thick oxide sur-

face are not discussed. Since nitridation can reduce the oxygen exchange, further investigation is necessary. Once the reliability problem is solved, leakage current from thick oxide region can be reduced even further or thinner EOT stack can be employed to enhance the performance of thick oxide device with high-k layer stacking.

4. Conclusions

Potential reliability problems of stacking thin HfSiOx layer on thick SiO_2 region for multiple oxide application are investigated. Mobility and interface states are not affected, but TZDB, SILC, and NBTI characteristics suggest that the thin HfSiOx layer reacts with the underlying thick oxide layer and affect the reliability characteristics. Since the stacking of a high-k layer on thick oxide can be used to reduce leakage current or to enhance the performance of thick oxide devices, further optimization to minimize the reaction is necessary.

References

[1] P.Kirsch et al., J. Appl. Phys., 99, 023508, 2006.
[2] H.Alshareef et al., to be presented at VSLI symposium, 2006.
[3] S.B. Samavedam et al., IEDM, 2002, p. 433
[4] Z.B. Zhang et al., VSLI symposium, 2005, p.50
[5] S.C. Song et al., to be presented at VLSI, 2006.
[6] G.Bersuker, B.H.Lee, H.Huff, Workshop of Future Electronics, 2004.

Sample	A	B	C	D
Electrode	HfSix	HfSix	HfSix	TiN
$HfSiO_x$(Å)	30	30	30	0
Bottom SiO_2 (Å)	0	20	40	60
EOT(A)	14.4	26.9	46.1	60.1
V_{FB}(V)	-0.71	-0.71	-0.72	-0.70

Table.1 Multiple oxides stacks used in this paper. V_{fb} values of experimental group (HfSix electrode) match with TiN electrode.

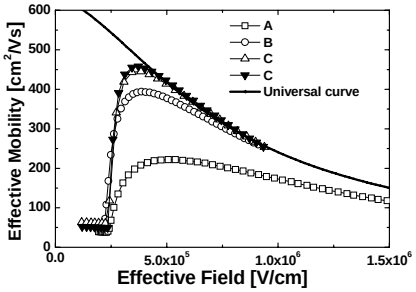

Fig.1 Mobility of samples shown in Table.1. $HfSiO_x$ layer affects the mobility when the underlying SiO_2 is thinner than 2nm.

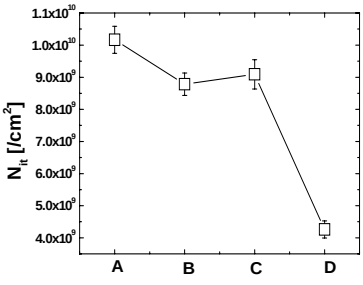

Fig.2 Nit is measured from NMOS region at frequencies ranging from 1KHz to 1MHz.

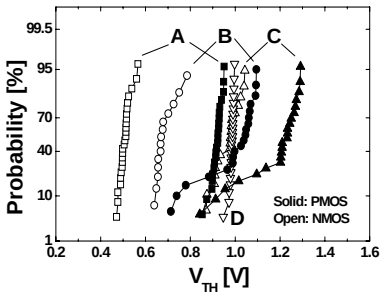

Fig.3 V_{th} distribution of NMOS and PMOS. Differences in Vth value is due to the EOT difference shown in Table.1.

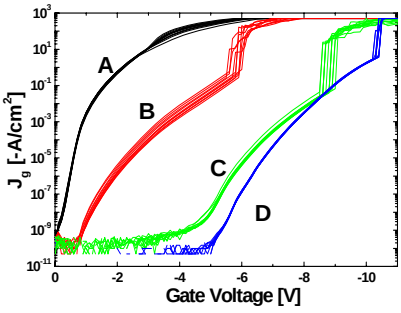

Fig.4 J-V curve showing breakdown characteristics of 200μm² capacitors. Small area capacitor is used to observe the intrinsic breakdown characteristics.

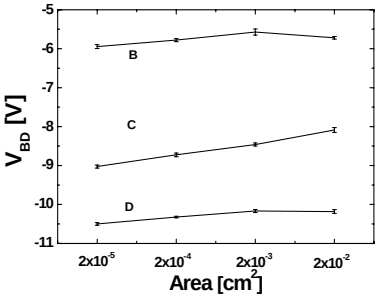

Fig.5 Area dependence of TZDB characteristics. Negligible area dependence indicates the TZDB characteristics are intrinsic.

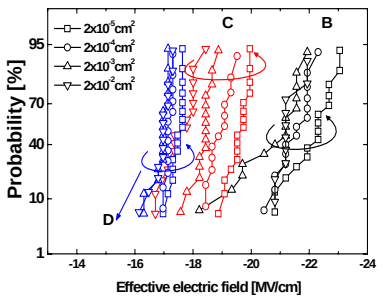

Fig.5 Weibull plot of breakdown field under TZDB stress. Device A is excluded due to indistinct breakdown.

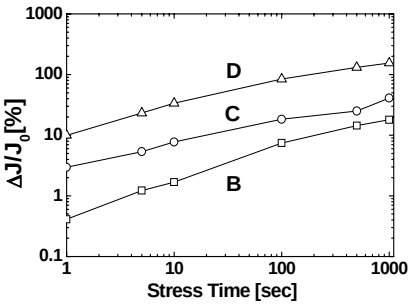

Fig.7 SILC characteristics of $HfSiO_x/SiO_2$ stack. All samples are stress at 12MV/cm. $HfSiO_x$ layer improves SILC characteristics in comparison with TiN/SiO_2 sample.

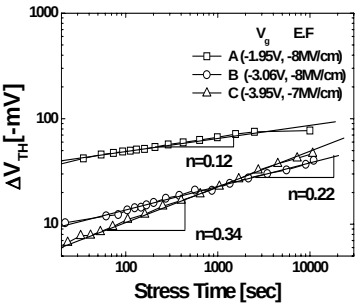

Fig.8 NBTI characteristic of $HfSiO_x/SiO_2$ stack. Constant voltage stress of 7-8MV/cm is applied at 125°C to increase the amount of V_{th} shift.