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Leakage mechanism of ultrathin SiON gate dielectric

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Abstract

Leakage mechanism of ultrathin gate SiON dielectric is studied considering dangling-bonds in the dielectric. The calculated and measured J_G-EOT characteristics are compared. Additionally, larger flat band shift in pMOS is studied using the first principles method.

Keywords: N≡Si_3, SiON, dangling-bond, TAT, and thin EOT

Introduction

Ultrathin SiON film is a candidate for next gate dielectric, because the improvement of fabrication process has decreased equivalent oxide thickness (EOT) and gate leak [1], suppressed boron penetration [2] and flat band shift (ΔV_{FB}) [3], and removed interfacial roughness [1]. However, still unclear is why ΔV_{FB} is larger in pMOS, as shown in Fig. 1. We will solve this problem and then study how dangling-bond (DB) affects the gate leak through the SiON dielectric.

Alloy Structure of SiON

Fig. 2 shows the ternary component diagram of SiON that is composed of $[(SiO_2)_{1-X}(Si_3N_4)_X]_{1-Y}Si_Y$ including interfacial transition (IFT) layers, in which energy gap (EG), dielectric constant (K), valence band affinity (VBA) are changed from in Si to at the edges of the dielectric [4-6]. Throughout the dielectric, physical quantities (Q) are dependent of Si-N bond rate (R) [7, 8] but not of [N] [9] as follows: (Q in SiON) = (1–R) $\times Q_{OX}$ + R$\times Q_{SiN}$, where R=3X/ (1+2X) and X=0.75[N]/ (1-[N]). The profiles of [N] and [O] are measured by AR-XPS method. We can then extract R, EG, K, VBA, IFT layer widths (W_{IFT}), and tunnel masses of electrons and holes (m_e and m_h) from the measured [N]-profile by using the values for Q in SiO_2 and Si_3N_4 (Q_{OX} and Q_{SiN}, respectively) in Table 1. Fig. 3(a)-(d) depicts the results of a measured sample.

Analysis of dangling-bonds and flat band shift

In Fig. 4, the first principles calculation shows that N-atom incorporated in Si (100) causes Si dangling bonds (Si-DB). In Fig. 5, the upper insertion depicts Si-DB and 2-fold N dangling-bond (N-DB) in the Si energy band [3]. A combined trap distribution of these DBs has a broad tail in the density-of states (DOS) diagram. According to [10], the center of the combined distribution (E_T) is assumed to be at the level lower from the Si mid-gap by 0.4eV at the interface. The half-value width (0.1eV [10]) of the distribution can be extended with ΔE_T (z) =0.1eV×EG (z)/1.12eV, where z is a position in space through the dielectric and EG (z) is shown in Fig. 3 for example. In Fig. 6, the positive charge is contributed by upper tail above the Fermi level (E_F) at each bias condition, and then causes the V_{FB} shift and tunnel barrier modulation. Since the upper tail is composed mainly of Si-DBs, the V_{FB} shift and the barrier modulation can be ascribed to the Si-DBs.

Dividing the film into grids (i=1, 2…M) and integrating the Poisson equation, we have $K_i \varepsilon_0 \Delta V_i / \Delta T_i = -q\Delta N_i$, where ε_0 is the vacuum permittivity, q is the elementary charge, and ΔT_i is the width of i-th grid layer. ΔN_i and ΔV_i are the number of trapped charges of i-th grid layer and potential drop due to ΔN_i, respectively. K_i is the dielectric constant of i-th grid layer. Integrating these grid layers, we have $\Delta V_{FB}=\Sigma\Delta V_i = -(q/M/\varepsilon_0)\ \gamma T_{phys}$, where $\gamma = \sum\Delta N_i / (3.6R_i - 3.9)$ and T_{phys} is a physical thickness of dielectric film. Since only a portion of Si-N bonds gives trap site, we cannot directly extract ΔN_i from the measured R-profile. Then, we assume that the trap density (N_T) is equal to $Y_{DB}\times$R, where Y_{DB} is the dangling-bond (trap site) yield from Si-N bonds. In Fig. 7, Y_{DB} is extracted to reproduce V_{FB} in measured CV characteristics and the resultant values are summarized in Table 2. Note that Y_{DB} in pMOS is 2-times larger than in nMOS, which is equivalent to the behavior of ΔV_{FB} in Fig. 1. In pMOS, larger ΔV_{FB} is therefore ascribed to larger Y_{DB}.

Calculation of gate leakage current

Fig. 8 depicts the impact of barrier modulation estimated as tunnel barrier change from that of Y_{DB}=0 (no positive charge). This modulation increases the barrier for holes and lowers that for electrons, and is also dependent of bias condition, as schemed in Fig. 6.

On the other hand, m_h has been unknown, while m_e was extracted to be $0.85m_0$ with including the IFT layers [4], where m_0 is the rest electron mass. To extract m_h, we compare calculated and measured currents of samples in which the [N]-profile is uniform [12], as shown in Fig.9. There exist cross points in currents between electrons and holes, since the increase of [N] substantially reduces VBA, that is, tunnel barrier for holes, from 4.49eV to 1.9eV (See Table 1). It is found that the calculated cross points are agreed with the measured one while $m_e=m_h=0.85m_0$.

Trap-assisted tunneling (TAT) current is calculated by integrating the product of: (1) capture cross-section of traps (σ), (2) N_T (z), and (3) 2-step tunneling probabilities of electrons and holes [11]. The integration is carried out with space (z) and energy (E). The gate current density (J_G) is then calculated by adding this to the direct tunneling current of electrons and holes that aren't captured by any traps. In Fig. 10, TAT disappears while the capture radius is in atomic scale.

Results

Taking into account $m_e=m_h=0.85m_0$, the tunnel barrier modulation, the measured [N]-profile, the extracted Y_{DB}, and regarding σ as a fitting parameter, we compare the CV-JV curves between experiments and theory. An excellent agreement is obtained when $\sigma = 0$, as shown in Fig. 11. The leakage mechanism is therefore direct tunneling affected by positive charges trapped by Si-DBs. In Fig. 12, we compare the calculated and measured J_G-EOT characteristics. To suppress the gate leak, nMOS requires larger Y_{DB} because T_{phys} increased for a given EOT overcomes the barrier lowering (shown in Figs. 6 and 8) partially increasing the electrons current. In opposite, pMOS requires smaller Y_{DB} because T_{phys} increased for a given EOT overcomes the reduction of the barrier increasing for holes (shown in Figs. 6 and 8). Additionally, B atoms of p^+poly-Si can generate B-N-B cluster in the dielectric. Since this cluster is mobile even in β-Si_3N_4 in which the cluster is more stable than in SiON [18], the extrinsic Si-DB is left after the cluster has gone, as shown in Fig. 13. Therefore, pMOS has the extrinsic Si-DBs as well as the intrinsic Si-DBs generated before fabricating the gate poly-Si, while nMOS has only the intrinsic Si-DBs.

Conclusion

If Y_{DB} is controlled, smaller EOT and smaller gate leak can be realized. We are required to obtain larger Y_{DB} in nMOS and smaller Y_{DB} in pMOS. Boron penetration from p^+poly-Si can generate the extrinsic Y_{DB}, which results in larger ΔV_{FB} in pMOS. The leakage mechanism is the direct tunneling affected by Si-DBs.

References

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Table 1 Used Variable

Quantity (Q)	Q_{OX}	Q_{SiN}	Q_{Si}
K	3.9[16]	7.5[16]	11.7
EG (eV)	8.95 [13]	5.4 [15]	1.12
VBA (eV)	4.49 [14]	1.9 [15]	0
m_e (m_0)	0.85 [4]	0.85(*)	–
m_h (m_0)	0.85(*)	0.85(*)	–
W_{IFT} (nm)	0.4 [4-6]	0.5 [17]	–

(*) Present results (Fig. 9)

Table 2 Extracted parameters

Sample	EOT	0.78 nm	0.89nm	1.0 nm
	Type	pMOS	nMOS	nMOS
Y_{DB}		1.5E–3	7.5E–4	7.5E–4

Y_{DB} in pMOS is 2-times larger than that in nMOS.

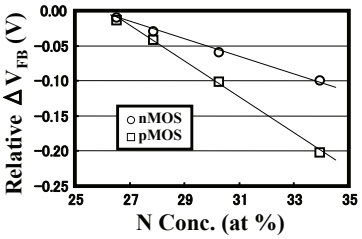

Fig. 1 Relative measured V_{FB} shift

Derivative in pMOS is 2-time larger than in nMOS.

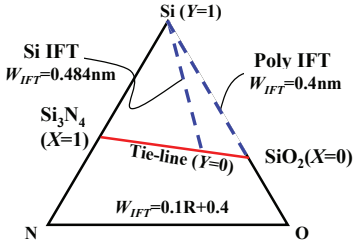

Fig. 2 Ternary component diagram of SiON

W_{IFT} is dependent of R. Tie line is on Y=0 (away from IFT layers).

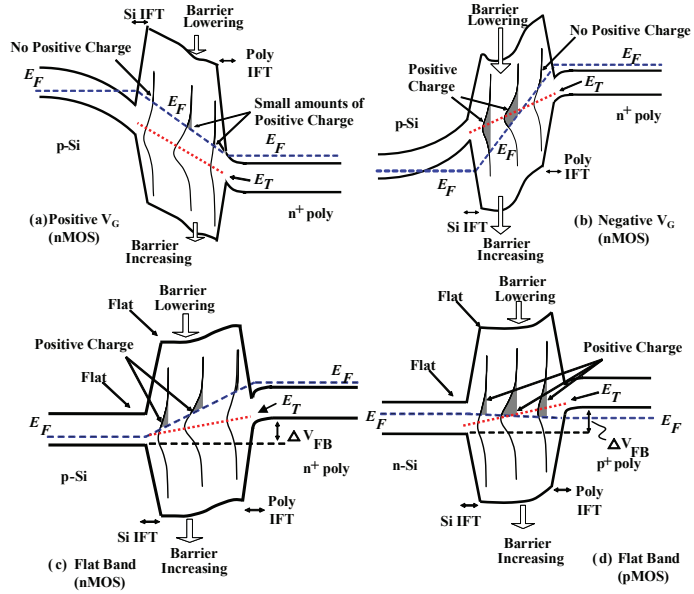

Fig. 6 Schemes for Trapped Positive Charge

The modulation of EG profile shown in Fig. 3 was omitted for ease of drawing in this figure. If this modulation is considered, the barriers for electrons and holes are further lowered and partially lowered, respectively. Of course, such an impact of EG modulation on the barrier modulation is considered in the calculation.

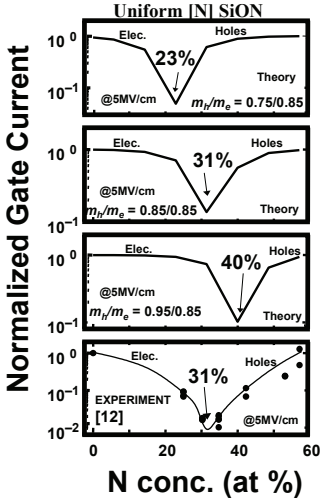

Fig. 9 Tunnel mass for holes

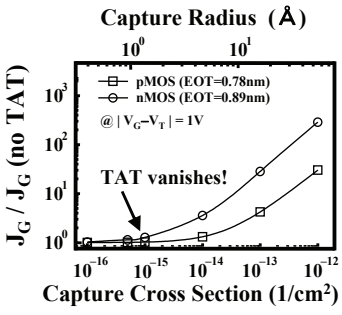

Fig. 10 Impact of TAT on J_G

TAT of holes is considered as well as that of electrons. The barrier modulation is considered and $m_e = m_h = 0.85m_0$ is used in the calculation.

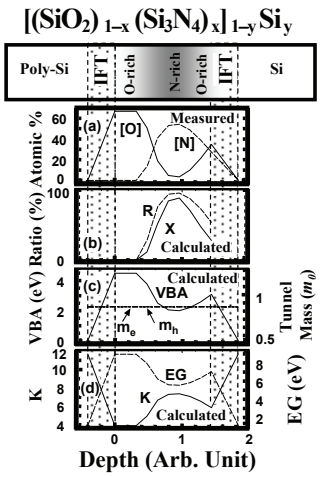

Fig. 3 Profiles of SiON dielectric of a measured sample

EG and K are changed with [N] and [O] through the dielectric film including the IFT layers. Physical thickness (T_{phys}) is a distance between the centers of IFT layers [4].

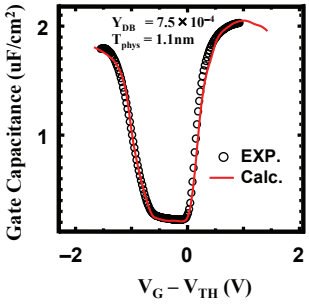

Fig. 7 CV-fitting to extract Y_{DB}

Y_{DB} is determined to reproduce V_{FB}.

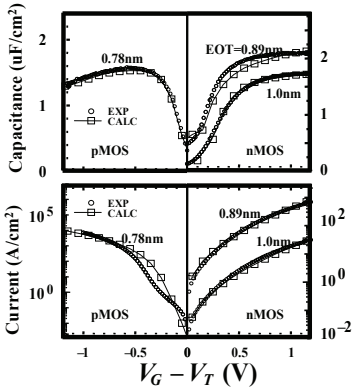

Fig. 11 CV-JV fitting

Impurity density profiles measured by SIMS are used in the calculation. All the CV-JV characteristics are calculated using the Poisson-Schrödinger solver developed by adding the present DB model to that used in [4].

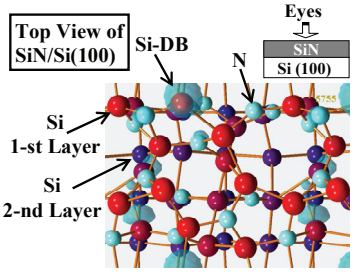

Fig. 4 First principles result of Si-DB due to incorporating N in Si (100)

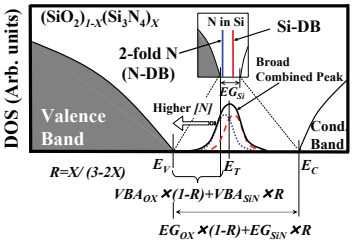

Fig. 5 Model for trap levels in SiON

VBA_{OX}, VBA_{SiN}, EG_{OX}, EG_{SiN} and EG_{Si} are from the literature (Table 1).

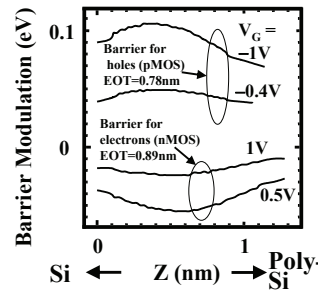

Fig. 8 Barrier modulation from Y_{DB}=0

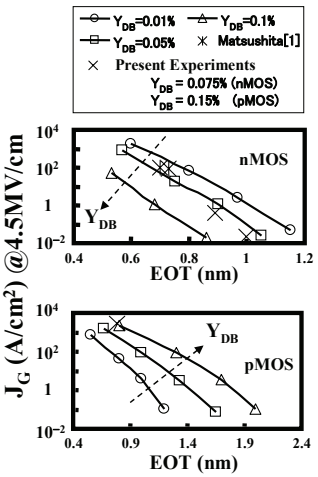

Fig. 12 Impact of Y_{DB} on J_G-EOT

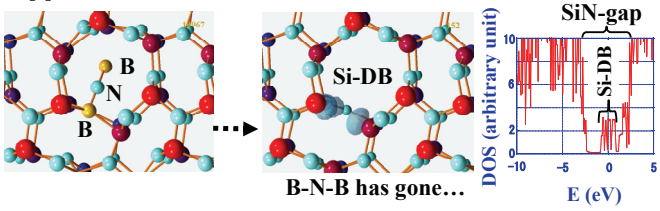

Fig. 13 Generation of extrinsic Si-DB from B-N-B cluster in β-Si_3N_4