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Improvement of mobility and NBTI reliability in MOSFETs with ALD-Si-nitride/SiO_2 stack dielectrics and p^+-poly-Si gate

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1. Introduction

Nitridation of the thin gate-SiO_2 has been widely adopted in the modern CMOS technology in order to suppress boron penetration from the p^+- poly-Si gate and increase the oxide permittivity. However, nitrogen incorporation has been found to enhance the negative bias temperature instability (NBTI) of pMOS significantly [1]. The enhancement is found to relate with the N concentration near the SiO_2/Si surface [2-3]. Therefore, the ideal N distribution in the SiON film is 100%N in the upper layer and 0%N in the lower layer. Atomic layer deposition (ALD) of SiN on SiO_2 can realize such an N distribution, and excellent boron suppression and reliability characteristics have been demonstrated [4-5]. In this paper, their carrier mobility and NBTI characteristics are examined, and the advantage of the ALD stack as a suitable gate-dielectric for next generation is cleared.

2. Device fabrication

P^+-poly-Si gated p- and n-MOSFETs were fabricated using a standard CMOS process [6]. For the ALD stack, approx. 2.0nm SiN was deposited on 2.0nm base-SiO_2, followed by post-deposition-annealing. For the SiON film, approx. 3.5nm base-SiO_2 was plasma-nitrided to introduce nitrogen with 14% peak concentration. The devices had suffered a heavy thermal budget of 750°C annealing for 60min peculiar to the DRAM fabrication process. The equivalent oxide thicknesses (EOT) of pMOS with SiN/SiO_2, SiON, and pure-SiO_2 dielectrics are 3.9, 3.0 and 3.5nm, respectively, as extracted from the accumulation capacitance. EOT of the corresponding nMOS is approx. 0.2nm thicker due to the poly-Si depletion effect.

3. Results and discussion

Fig. 1 shows the I_d-V_g curves measured at $|V_d| = 50$mV for devices with W/L = 10μm/10μm. V_{th} shifts to positive significantly for the SiO_2 and SiON devices compared to the ALD-SiN/SiO_2 devices. While, the n^+-poly-Si gated devices have similar V_{th} (not shown here). Therefore, the positive V_{th} shift in Fig. 1 can be ascribed to the boron penetration caused by the heavy thermal budget. As expected, the SiN/SiO_2 stack can suppress the boron penetration more effectively than the plasma-nitrided SiON film.

Figs. 2 and 3 show the DCIV curves measured at $|V_s| = |V_d| = 0.3$V on devices with area of $1.2\times10^5\mu m^2$. The interface trap density (N_{it}) of pMOS extracted from the DCIV peak height is approximately 0.57, 0.66, and 1.42×10^9 cm^{-2} for the ALD stack, plasma-nitrided-SiON, and pure-SiO_2 devices, respectively. For nMOS, the corresponding N_{it} is 1.08, 1.21, and 11.5×10^9 cm^{-2} respectively. For both p- and n-MOSFETs, the ALD stack devices have the lowest N_{it} value, and the pure-SiO_2 devices have the largest N_{it} value. It indicates that the boron penetration can increase the interface trap density, especially for the n-MOSFETs.

Figs. 4 and 5 show the electron and hole mobility extracted from the n- and p-MOSFETs using the split C-V method. In consistence with the N_{it} data, the ALD stack devices have the highest carrier mobility and the pure-SiO_2 devices have the smallest mobility. For hole mobility, the difference is small due to the relatively small difference in N_{it} (about 2 times). For the ALD stack without the heavy thermal budget, the hole mobility was reported to identical as the pure-SiO_2 ones [7]. On the other hand, the difference of electron mobility is quite large due to the significant difference in N_{it} (about 1 order of magnitude). Moreover, for the SiON devices, the effect of a long-range dipole field of the Si-N bonds near the SiON/Si interface may also reduce the electron mobility besides N_{it} [8].

Fig. 6 shows the time evolution of ΔV_{th} of pMOSFETs under NBT stress. For the SiON and pure-SiO_2 devices, ΔV_{th} is negative and approximately obeys the power-law dependence with the exponent around 0.25. Such a negative ΔV_{th} under NBT stress has been widely attributed to the interface trap and/or positive charge generation originated from dissociation of Si-H bonds at the SiO_2/Si interface [3]. Taking the V_{th} difference into account, NBTI of the SiON devices is much larger than that of the pure-SiO_2 ones, which has been ascribed to the higher density of the defect precursors (Si-H bonds) at the SiON/Si interface [2]. On the other hand, the ALD stack device shows an abnormal NBTI behavior: V_{th} shifts to positive at the beginning of stress, and then shifts to negative. The value of ΔV_{th} at the longer stress times is close to that of the pure-SiO_2 ones.

The initial positive jump of ΔV_{th} is more obvious for the smaller EOT ALD-stack devices. Fig. 7 shows the time evolution of ΔV_{th} of ALD-2.0nm-SiN/0.5nm-SiO_2 devices under NBT stress with different V_g. Fig. 8 shows the corresponding interface trap generation. The initial positive ΔV_{th} jump increases with $|V_g|$, and the negative ΔV_{th} rate at the longer stress times also increases. On the other hand, ΔN_{it} increases continuously with time approximately following the power-law dependence but with the exponent increasing with $|V_g|$. The above phenomena suggest there are electron traps in the stack film, most probably at the SiN/SiO_2 interface. The traps are neutral before stress, while can be occupied by electrons tunneling from the gate under the negative V_g bias to make ΔV_{th} positively shift, as shown in Fig. 9. Meanwhile, the degradation at the SiO_2/Si interface (to make ΔV_{th} negatively shift) is similar to that of the pure-SiO_2 device due to the absence of N in the interface. While, the negatively charged bulk traps can enhance the electrical field at the SiO_2/Si interface, resulting in faster degradation rate at higher $|V_g|$ for the ALD stack device. At low $|V_g|$ (real operation voltage), on the other hand, the neutralization effect may make its net ΔV_{th} even smaller than that of the pure-SiO_2 device.

In conclusion, we clearly show that the ALD stack gate

dielectrics offer the lowest interface trap density and highest carrier mobility compared with the SiON and pure-SiO_2 gate-dielectrics due to the effective suppression of boron penetration by the 100%N in the upper SiN layer. The 0%N at the SiO_2/Si interface makes its NBTI is somewhat similar to that of the pure-SiO_2 except an initial positive ΔV_{th} jump due to electron trapping in the SiN/SiO_2 interface. Therefore, the ALD stack is a very promising gate-dielectric.

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References

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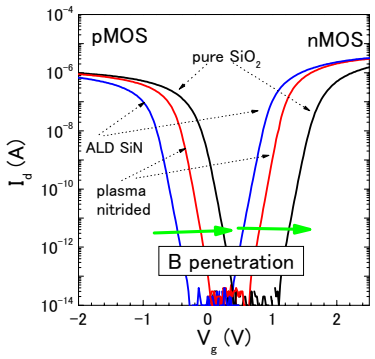

Fig. 1 I_d-V_g curves of p- and n-MOSFETs Devices with W/L=10μm/10μm measured at |Vd|=50mV.

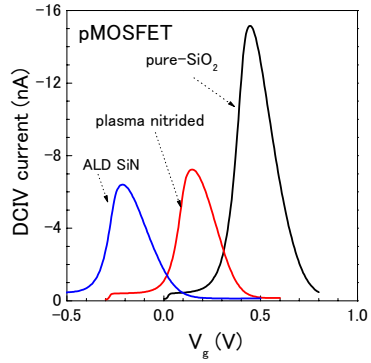

Fig. 2 DCIV curves of a pMOSFETs with ALD SiN/SiO_2 stack, plasma-nitrided SiON, and pure-SiO_2 gate-dielectrics. Devices with A=1.2×10^{5}μm^2 were measured at V_s=V_d=-0.3V.

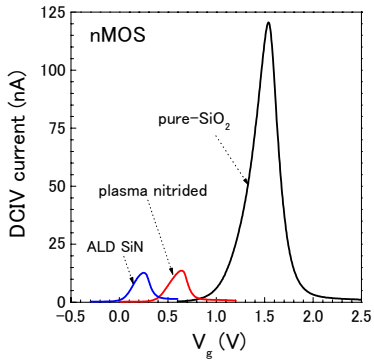

Fig. 3 DCIV curves of a nMOSFETs with ALD SiN/SiO_2 stack, plasma-nitrided SiON, and pure-SiO_2 gate-dielectrics. Devices with A=1.2×10^{5}μm^2 were measured at V_s=V_d=0.3V.

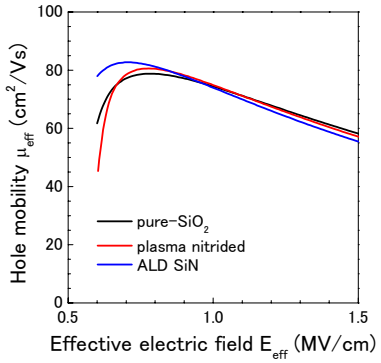

Fig. 4 Hole mobility extracted using a split C-V method for devices with ALD SiN/SiO_2 stack, plasma-nitrided SiON, and pure-SiO_2 gate-dielectrics.

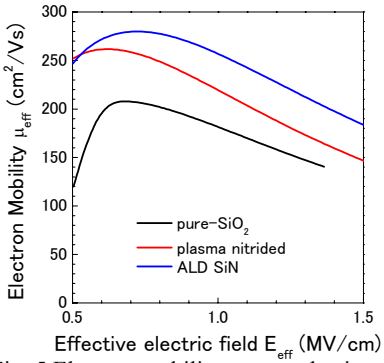

Fig. 5 Electron mobility extracted using a split C-V method for devices with ALD SiN/SiO_2 stack, plasma-nitrided SiON, and pure-SiO_2 gate-dielectrics.

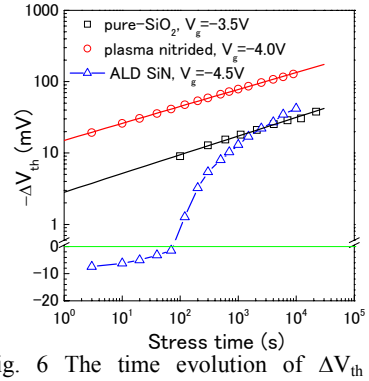

Fig. 6 The time evolution of ΔV_{th} for pMOSFETs with various gate-dielectrics under NBT stress at T=125°C and $|V_g-V_{th}| \approx$ 3.8V. The solid lines are fitting lines based on the power-law dependence. The exponent is around 0.25.

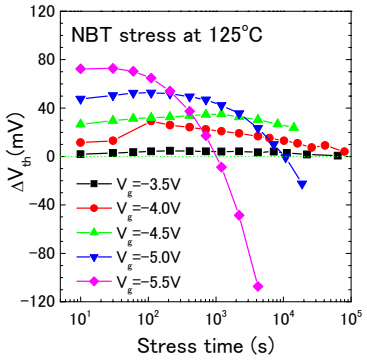

Fig. 7 The time evolution of ΔV_{th} for pMOSFETs with the ALD SiN/SiO_2 stack gate-dielectrics under NBT stress with V_g from -3.5V to -5.5V.

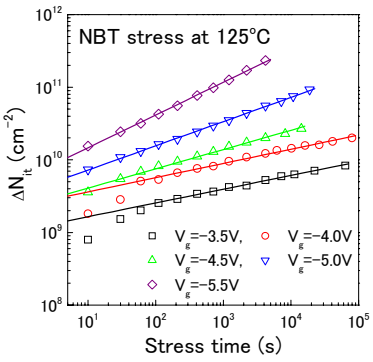

Fig. 8 The time evolution of the corresponding ΔN_{it} extracted from DCIV. The solid lines are fitting lines based on the power-law dependence. The exponent increases slightly with $|V_g|$ increasing.

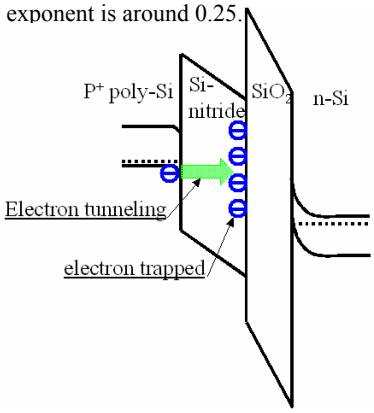

Fig. 9 Illustration of band diagram of the SiN/SiO_2 stack under negative bias showing the existence of electron traps at the SiN/SiO_2 interface, which can be occupied by electrons tunneling from the gate.