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Electrical characteristic improvement of high-k gated MOS device by nitridation treatment using plasma immersion ion implantation (PIII)

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1. Introduction

The research topics of high-k gate dielectric processes are the key technology for the nano-scale MOS device in IC. The nitridation treatments on silicon surface and ultra-thin gate dielectric are very important for these researches [1]. To improve the electrical properties and the thermal stability of high-k gated MOS devices, the optimal surface nitridation at silicon surface should be developed. This is because the diffusion of impurity in gate dielectric can be clearly suppressed and the interfacial oxide formation from the out-diffusion of oxygen in Si wafer can be decreased by a nitridation treatment at Si surface [2]. Thus a nitridation treatment at Si surface followed by high-k deposition is helpful to improve the thermal stability and decrease the interfacial oxide formation. Recently, plasma immersion ion implantation (PIII) is a promising technique for atom incorporation [3,4], which possesses several advantages such as high-dose, shallow depth, low damage, high-dose range, and precise depth, etc. Therefore, the nitridation at silicon surface by PIII and the nitrogen incorporation on the electrical properties of MOS devices with high-k gate dielectric deserve to investigate. In this work, the nitridation at silicon surface by PIII and the electrical characteristic improvement of high-k gated MOS devices have been studied. The physical correlation between nitrogen concentration profile at Si surface and the electrical properties of MOS devices is discussed as well.

2. Experimental

MOS capacitors fabricated in this work were $TaN/HfO_xN_y/Si$ structures. A screen oxide was formed on some wafers before nitrogen implantation. The ion energies for PIII were 5 kev ~ 20 kev and the implantation times for it were 5~60 min. An annealing was performed at 850 ^oC after PIII. The HfxNy (~2.0 nm) gate dielectric was deposited by a reactive dc magnetron sputtering with 99.99% pure Hf target in Ar/N2 = 24 /36 sccm, Power = 100 W, Pressure = 7.6 mTorr. Then, a post-deposition-anneal (PDA) at 850 ^oC in N2 gas for 30 s was performed to form HfOxNy (~4.5 nm).

3. Results and Discussion

Fig. 1 shows C-V curves for high-k gated MOS devices with Si surface nitridation by PIIII at two energies, indicating the interface quality is satisfactory. Fig. 2 depicts the leakage current density and effective oxide thickness (EOT) for high-k gated MOS devices with various Si surface nitridation. The leakage current density for samples with Si surface nitridation by PIII is clearly lower than the other ones. Besides, the EOT for samples with Si surface nitridation by PIII is slightly thicker than those by thermal process. The hysteresis-induced flatband voltage shift ΔV_{FB} for high-k gated MOS devices with various nitridation at Si surface is shown in Fig.3. The hysteresis is slightly increased for sample with surface nitridation. Fig. 4 shows interface trap density Dit for all samples. A lower Dit is obtained for sample nitrided by PIII at a low energy or using a screen oxide.

Fig. 5 illustrates the stress-induced flatband voltage shift (ΔV_{FB}) for high-k gated MOS devices with various nitridation at Si surface. It is clear that a decrease of ΔV_{FB} can be achieved by a rich thermal nitridation at Si surface. The stress-induced ΔV_{FB} for sample nitrided by PIII is kept at almost zero. It is also seen in Fig. 6 that stress-induced leakage current is significantly decreased by surface nitridation by PIII. Thus, the nitridation treatment at Si surface by PIII is a promising technique to improve the hot-electron-related reliability of high-k gated MOS device.

Based on the electrical characteristics mentioned above, MOS device with nitridation at Si surface by PIII at a lower energy and for a short time demonstrates clear improvement on reliability and Dit, and it shows comparable properties in EOT, leakage current, and hysteresis.

Fig. 7 plots the depth profiles of nitrogen for samples with Si surface nitridation by PIII at various ion energies and/or for various implantation times. It is clear that a higher ion energy or a longer implantation time results in a deeper profile. Contrarily, a low ion energy and a short implantation time for PIII can form a shallow depth profile.

3. Conclusion

In summary, the electrical characteristics of high-k gated MOS devices are improved by a nitridation treatment using PIII at a low ion energy and for a short implantation time. Experimental results suggest that a shallow nitrogen profile at Si surface is promising for further enhancement of device properties.

References

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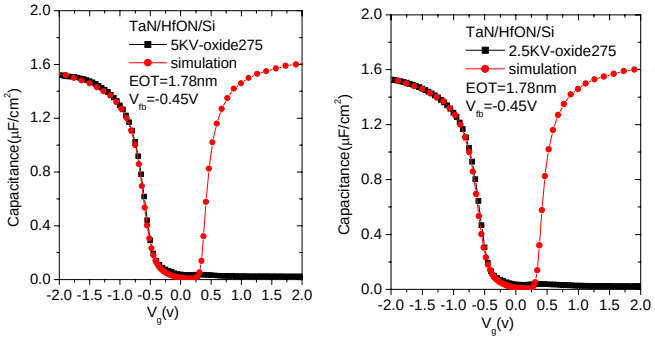

Fig. 1 C-V curves for high-k gated MOS devices with various nitridation at Si surface by PIII

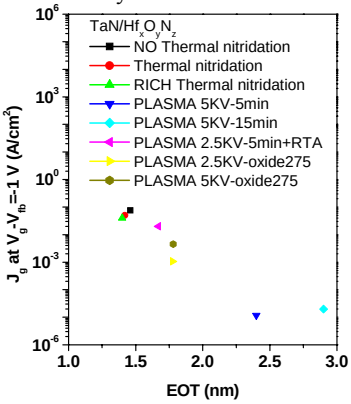

Fig. 2 The leakage current density and EOT for high-k gated MOS devices with various nitridation at Si surface

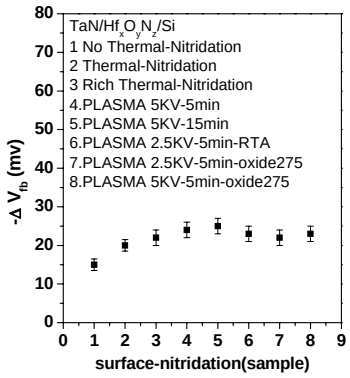

Fig. 3 The hysteresis-induced flatband voltage shift ΔV_{FB} for high-k gated MOS devices with various nitridation at Si surface

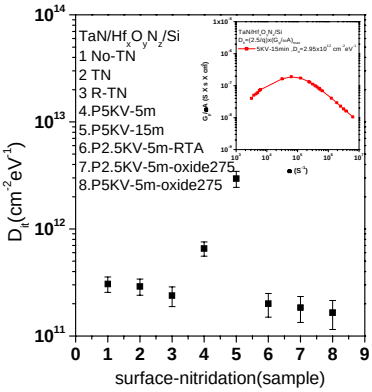

Fig. 4 The interface trap density Dit for high-k gated MOS devices with various nitridation at Si surface

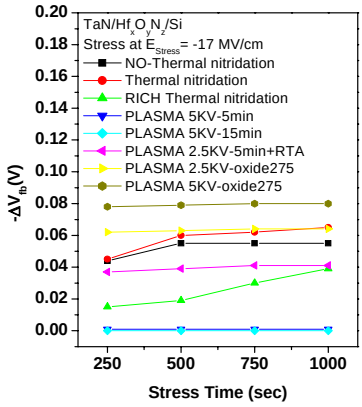

Fig. 5 The stress-induced flatband voltage shift ΔV_{FB} for high-k gated MOS devices with various nitridation at Si surface

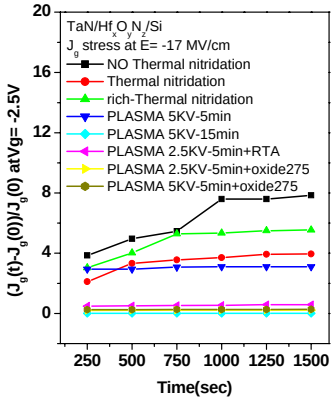

Fig. 6 The stress-induced leakage current (SILC) for high-k gated MOS devices with various nitridation at Si surface

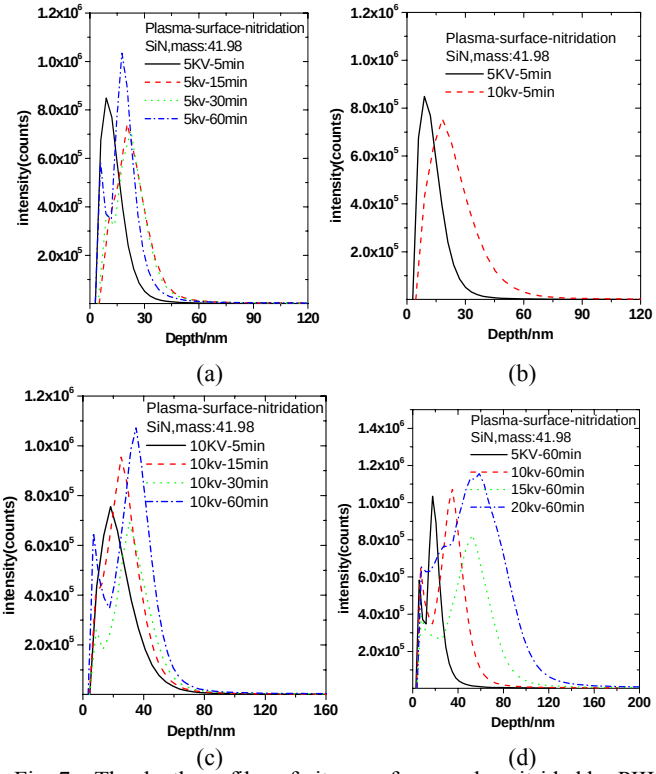

Fig. 7 The depth profiles of nitrogen for samples nitrided by PIII (a) at 5 kV for various time, (b) at 5 kV and 10 kV for 5 min, (c) at 10 kV for various time, and (d) at various energies for 60 min, analyzed by secondary ion mass spectroscopy (SIMS).