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Effect of Gate Oxide Thickness Uniformity on the Characteristics of Three-dimensional Transistors

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1. Introduction

With the shrink of DRAM devices below sub-100nm regime, several 3-dimensional (3D) cell transistors and dual poly-Si gate process have been widely studied to improve the data retention characteristic that is the key parameter of DRAM devices and to improve transistor performance at low operation voltage, respectively. The 3D cell structure such as recess-channel gate (RG) [1,2] involves several Si surfaces with different crystal orientations within the channel as shown in Fig. 1. The different crystal planes result in the different silicon oxidation rates from point to point within the channel. The several gate oxide thicknesses in the recess channel cause RG cell transistor to have quite different characteristics compared to conventional planar transistor. Like the different oxidation behavior in 3D structure, the effect of the nitridation of the gate oxide in recess channel plane by plasma nitridation, which is inevitable to suppress boron penetration from boron doped poly-Si in PMOSFETs, is also considered to be different from that of planar transistor.

In this paper, we observed the gate oxide profile within the RG cell with several oxidation methods and also investigated the nitridation behavior of the RG gate oxide. The effect of the gate oxidation methods was evaluated by characterizing the reliability and the transistor performances of the RG cell transistor.

2. Experimental

Using the 80nm DRAM technology, the RG cell transistor was fabricated on the p-type (100) Si substrate with the (110) flat zone. The recess depth is 120nm and the bottom of the recessed channel is well rounded as shown in Fig.1 (a) and (b). The source/drain junction depth of the cell transistor is about 100nm. To investigate the effect of gate oxide thickness profile in the RG structure on the cell transistor reliability, we performed the dual gate oxidation process with three combinations using dry oxidation and radical oxidation; dry-dry, radical-radical, and dry-radical. Plasma nitridation was then performed to suppress boron penetration in PMOSFETs.

3. Results and Discussion

In order to investigate the effect of gate oxide thickness along the RG sidewall, we prepared three samples by changing the oxidation methods during the dual gate oxidation process. Fig. 1 compares the gate oxide profile in RG structure. Even though the gate oxide thicknesses of Si top surface (S) and bottom region (B) are identical for three samples, those along the recess Si plane are quite different. Compared to the other samples, the radical-radical sample exhibits the lowest oxide thickness along the sidewall plane due to its immunity to crystal orientation. The dry-radical sample shows gate oxide thickness slightly lower than that of dry-dry one.

Figure 2 shows the cross-sectional TEM image and the N k-edge spectrums by electron loss near edge spectroscopy (ELNES) at RG cell after plasma nitridation of the dry-radical gate oxide. N peak is observed at ~401eV regardless of positions, indicating that nitrogen is piled-up even at the sidewall and the bottom gate oxide. In order to check the plasma nitridation characteristics in RG structure, we prepared both planar and RG MOS capacitors having three different gate oxide thicknesses by dry-radical combination and compared the change of capacitances. Figure 3 displays the relationship between two structures and the plasma nitridation effect. The slopes before and after plasma nitridation are almost identical. The capacitance increase by plasma nitridation in the RG cell is about 93% of that in the planar cell. These behaviors suggest that nitridation is retarded at the 3D structure due to a geometry effect.

Figure 4 displays the C-V curves of RG cell array as a function of oxidation method. The difference in the accumulation capacitances is attributed to the different gate oxide thickness in RG structure as shown in Fig. 1. Figure 5 shows TDDB characteristic under constant current stress at RG cell array. Radical-radical sample exhibits superior reliability. It is interesting that the Weibull slope and the reliability of dry-radical sample is much improved compared to the dry-dry one. It is well known that the radical oxidation improves the reliability of gate oxide. One of other reasons for the improvement by radical oxidation is related to the oxide thickness profile along the sidewall plane. The gate oxide is the thickest at the sidewall region and the thinnest at the bottom region due to its crystal orientation, which results in a non-conformal electric field along the gate oxide. The non-conformal electric field is considered to be severer as the gate oxide thickness uniformity along recess-channel plane is worse.

Figure 6 exhibits the gate-induced drain leakage (GIDL) characteristics of RG cell array. The GIDL is known as band-to-band tunneling current in a deep depletion layer at gate-junction overlap and it depends on the gate oxide thickness at the gate electrode edge [3]. Like the dependence of GIDL on the oxide thickness in gate-junction overlap in planar transistor, the varying oxide thickness along the sidewall plane in the RG structure as shown in Fig. 1 (c) is believed to strongly affect the GIDL characteristic.

Shown in Fig. 7 are the Vg-Id and Gm curves of RG unit cell transistors measured before and after the GIDL stress (Vd=8V). The Id and Gm of fresh samples are shown to depend on the gate oxidation method, where the dry-dry sample displays the worst performance and the radical-radical one is the best. After the GIDL stress, the degradation behaviors of Id and Gm are also dependent on the oxidation method. Considering the RG cell structure, a deep depletion layer in the high drain stress, touching the source/drain junction, is expected to be developed at the RG top corner and the sidewall region. The high drain stress (Vd=8V) is able to generate some traps within the SiO_2 and/or at the SiO_2/Si interface at the RG top corner and the sidewall region. Therefore, the degradation under GIDL stress is related to the difference in the oxide thickness along the side wall plane; the thinner the gate oxide thickness along the recess-channel plan is, the worse the degradation is.

4. Conclusion

We investigated the oxidation and nitridaton behaviors within the 3D RG cell transistor. The gate oxide thickness uniformity in the RG is improved by introducing the radical oxidation. The nitridation efficiency of the gate oxide in the RG cell is decreased compared to the planar cell due to the 3D geometry effect. The conformal gate oxide in the RG cell by radical oxidation improves the TDDB characteristic of the gate dielectric and the transistor performance, whereas the GIDL is degraded by employing the conformal gate oxide at the sidewall, confirming that a trade-off exists.

References

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[2] J. Y. Kim *et al.*, Symp. on VLSI Tech., p. 11-12, 2003.
[3] Y. P. Kim *et al.*, IEEE Trans. Electron Devices, p. 104-108, 2001.

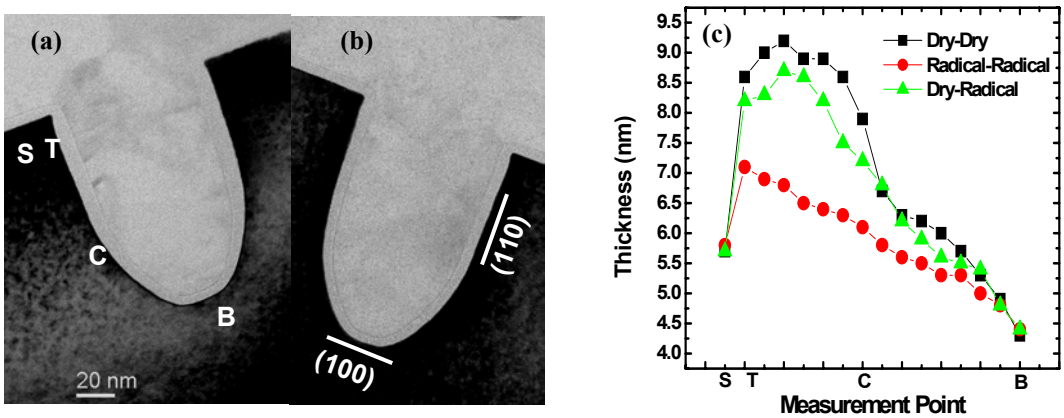

Figure 1. Cross-sectional TEM of recess-channel gate (RG) cell formed by (a) dry-day oxidation and (b) radical-radical oxidation. (c) Gate oxide thickness along the recess-channel plane for oxidation methods.

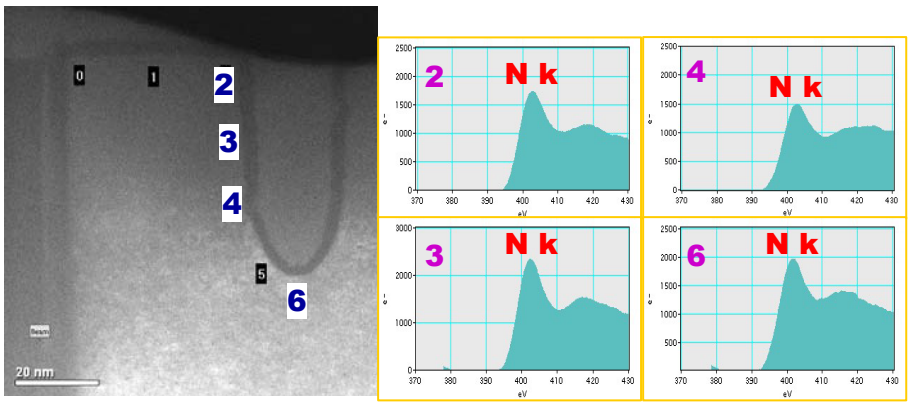

Figure 2. Cross-sectional TEM image of RG cell and N k-edge spectrums with each gate oxide point along recess channel plane by electron loss near edge spectroscopy (ELNES).

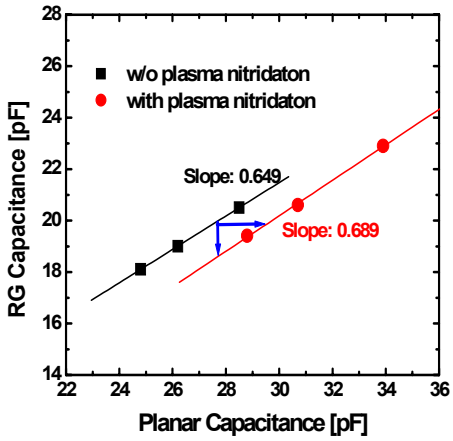

Figure 3. Capacitance comparison of planar and RG structures with and without plasma nitridation. Bigger planar pattern than the RG pattern was measured.

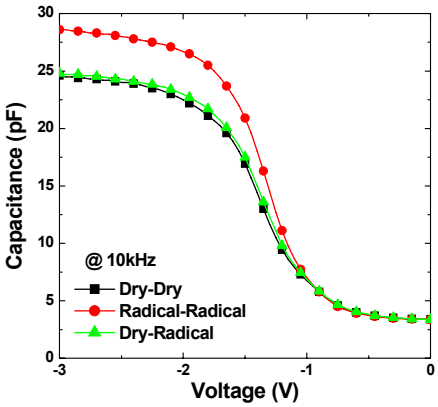

Figure 4. Capacitance of RG array structure as a function of oxidation method.

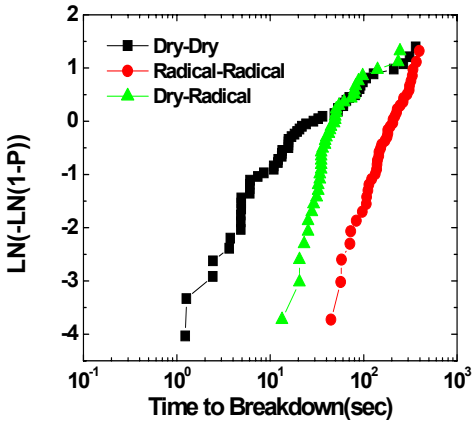

Figure 5. TDDB characteristics of RG array structure with oxidation methods.

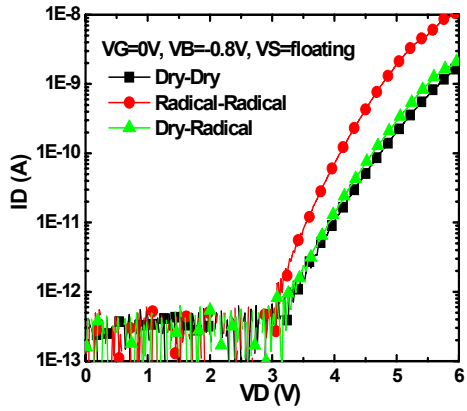

Figure 6. GIDL characteristics of RG cell transistor with oxidation methods.

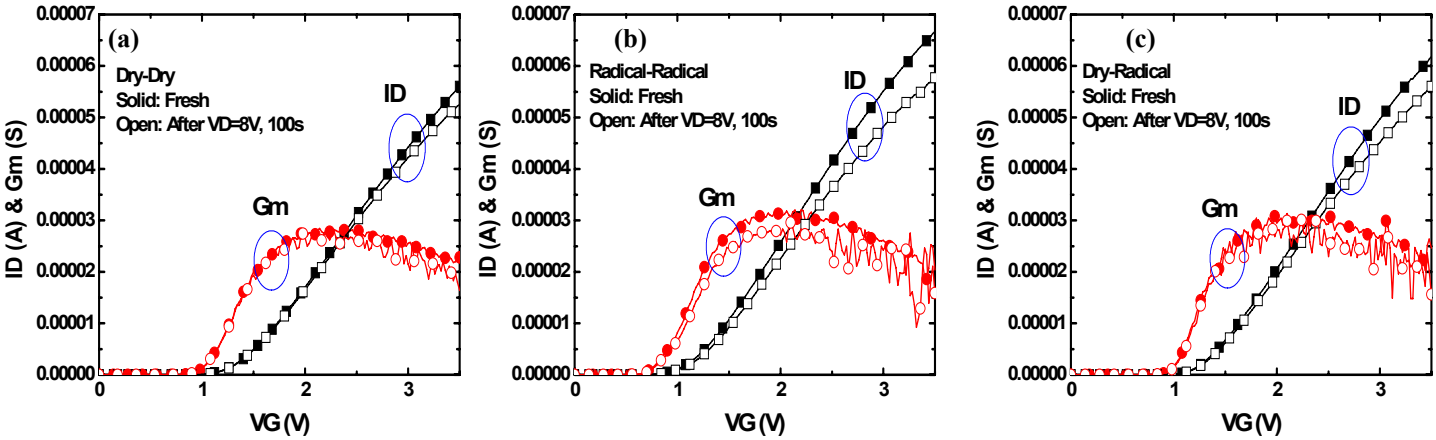

Figure 7. Vg-Id characteristics of the RG unit cell transistor before and after gate-induced drain leakage (GIDL) stress (Vd=8V, 100sec). (a) Dry-Dry, (b) Radical-Radical, and (c) Dry-Radical.